High Performance SEB Hardened Trench Power MOSFET with Partially Widened Split Gate and Trench Source

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***Abstract*—In this paper, an optimized trench power MOSFET is presented with three-dimensional (3D) TCAD simulation. A superior device's performance can be achieved by using the partially widened split gate and the trench source. Simulation results indicate that the new structure can present a good static parameters and a better $R_{DS(ON)}$×Q_{GD} FOM compared with the conventional structure. Moreover, the proposed structure shows no SEB under the device's rated breakdown voltage and the LET value of 1pC/μm (100MeV·cm^2·mg^{-1}, approximately the maximum LET energy of gold or bismuth ion). That means, the proposed structure will not exhibit SEB under heavy ions. Therefore, the new structure demonstrates a good electrical parameter and a superior SEB SOA simultaneously.**

Keywords—Trench power MOSFETs, single-event burnout (SEB), widened split gate, parasitic bipolar transistor

I. INTRODUCTION

The trench power MOSFETs are indispensable component in aerospace application, such as switching power supplies and DC-DC converters in the space power electronics system. When used at the high latitude region or space radiation environment, one of main destructive phenomenon that could cause the power MOSFETs permanent failure is Single-Event Burnout (SEB), which is triggered by the energetic ions[1-4].

Recent years, one of effect ways to improve the device characteristic is by using split gate concept in the trench power MOSFET, which can optimize the switching characteristic effectively due to the reducing of the gate-to-drain charge Q_{GD}[5]. To increase the device reliability without sacrificing other parameters, a partially widened split gate trench structure was presented in our previous research work[6]. It can enhance the SEB survivability effectively compared with the conventional trench structure. But the SEB safe operating area (SOA) cannot reach to the most safety situation in the previous proposed structure due to the occurring of the SEB behavior under a high drain bias voltage and a high LET value. Therefore, we try to enhance the SEB survivability further without sacrificing the device parameters.

In this paper, we present an optimized partially widened split gate power MOSFET with an appropriate trench source design. To investigate the device characteristics comprehensively, the electrical parameters are analyzed firstly, including the basic static parameters and the figure-of-merit (FOM) $R_{DS(ON)}$×Q_{GD}. Then, the SEB SOA are investigated and inner physical behavior are compared with three-dimensional (3D) TCAD simulation.

II. DEVICE STRUCTURE

Fig. 1 shows the cross-sectional view of the different structures. All structures are designed with the same N-type epitaxial layer thickness and doping concentration to achieve 200V rated breakdown voltage. As we mentioned in the previous structure [6], the gate structure is widened laterally below the N+ source region to suppress the parasitic bipolar transistor. Then, the source contact is etched with an appropriate trench depth, which can change form 0μm to 1.8μm, as shown in Fig 1(c). Obviously, the depth of 0μm is our previous structure selection. In this paper, we select the 0.8μm trench source depth as the baseline structure. The major structural parameters are shown in Table I. The simulations are performed by Synopsis Sentaurus Technology Computer Aided Design (TCAD) software.

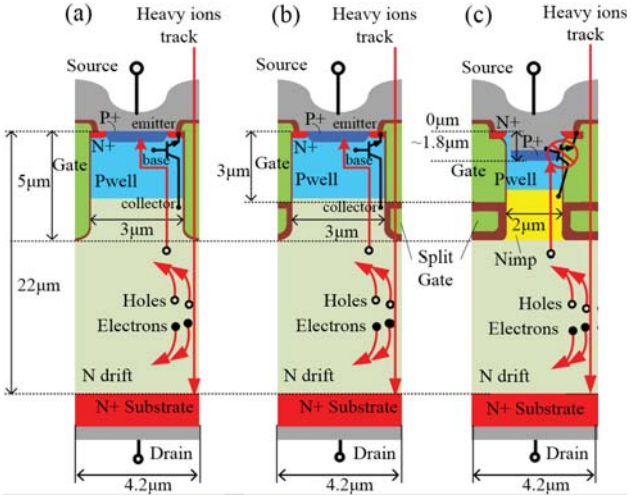

Fig. 1. Schematic cross-sectional view of (a) the conventional trench structure, (b) the conventional split gate structure and (c) the proposed structure. The trench source changes form 0μm to 1.8μm. the depth of 0μm is our previous structure.

III. DEVICE ELECTRICAL PARAMETERS AND SEB PERFORMACE

The breakdown voltage of the conventional structure, the split gate structure and the proposed structure at 100nA are 227V, 251V and 255V, respectively. The breakdown voltage of the proposed structure is higher than that of the conventional structure owning to the local RESURF effect near the split gate region [5]. The threshold voltage of three structures at drain current of 1mA are 3.51V, 3.51V and 3.33V, respectively.

The gate charge and forward I-V characteristic is given in Fig. 2. At a current density I_{DS} of 1A/mm^2 and V_{GS}=10V, the specific on-state resistance $R_{DS(ON)}$ of the conventional structure, the split gate structure and the proposed structure

978-1-7281-0286-3/19/$31.00 ©2019 IEEE

are 840mΩ•mm^2, 1091mΩ•mm^2 and 850mΩ•mm^2, respectively. The increasing of the $R_{DS(ON)}$ in the split gate structure is related to the local JEFT resistance at the split gate region. Therefore, we add the Nimp region at that region, as shown in the Fig.1(c). The gate-to-drain charge Q_{GD} of the conventional structure, the split gate structure and the proposed structure are 1.98nC/mm^2, 0.37nC/mm^2 and 0.34nC/mm^2, respectively. So, the figure-of-merit (FOM) $R_{DS(ON)}\times Q_{GD}$ of the conventional structure, the split gate structure and the proposed structure are 1663mΩ•nC, 404mΩ•nC and 289mΩ•nC, respectively. The FOM of the proposed structure is reduced by 82.6% compared with the conventional structure.

TABLE I MAJOR STRUCTURAL PARAMETERS

Structural Parameters	Conventional structure	Split gate structure	Proposed Structure
Cell pitch (μm)	4.2	4.2	4.2
N-drift thickness (μm)	22	22	22
Gate oxide thickness (nm)	100	100	100
Trench gate depth (μm)	5	5	5
Trench gate width (μm)	1.2	1.2	2.2
Mesa width (μm)	3	3	2
N-drift doping (cm^{-3})	1×10^{15}	1×10^{15}	1×10^{15}
P-well depth (μm)	2.8	2.8	2.8
P-well doping (cm^{-3})	1×10^{17}	1×10^{17}	1×10^{17}
N+ depth (μm)	0.3	0.3	0.3
N+ width (μm)	0.5	0.5	0.5
N+ doping (cm^{-3})	1.5×10^{20}	1.5×10^{20}	1.5×10^{20}
Nimp doping (cm^{-3})	-	-	1×10^{16}
P+ doping (cm^{-3})	3×10^{18}	3×10^{18}	3×10^{18}
trench Source depth (μm)	-	-	0.8
trench Source width (μm)	-	-	1.6

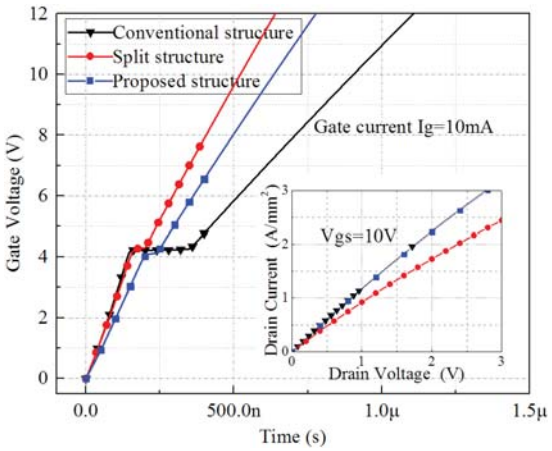

Fig. 2. Simulated gate charge and I-V characteristic for different structures. The curve of I-V characteristic is set at Vgs=10V.

To investigate the SEB behavior, the gate electrode is shorted with the source to ensure the MOSFET in the off-state. Then the drain bias voltage and LET value applied on the device are changed gradually to find the maximum critical value without SEB. The maximum drain bias voltage and LET value without SEB phenomenon are defined as the SEB threshold voltage and the critical LET value, which determines the SEB SOA.

Firstly, the bias drain voltage is set to increase with 5V steps at a fixed LET value. If the bias drain voltage reaches to rated breakdown voltage (200V for the simulated structure) without SEB, the LET value increases continually with 0.1pC/μm steps (for silicon material, 0.1pC/μm=10MeV·cm^2·mg^{-1}) to find the next critical drain voltage. If the LET value increases to 1pC/μm (100MeV·cm^2·mg^{-1}, approximately the maximum LET value of gold or bismuth ion) without SEB,[2],[8] we believe that the device will not exhibit SEB. Conversely, if the drain current or lattice temperature increases continually during the transient process, it indicates the occurring of SEB behavior.

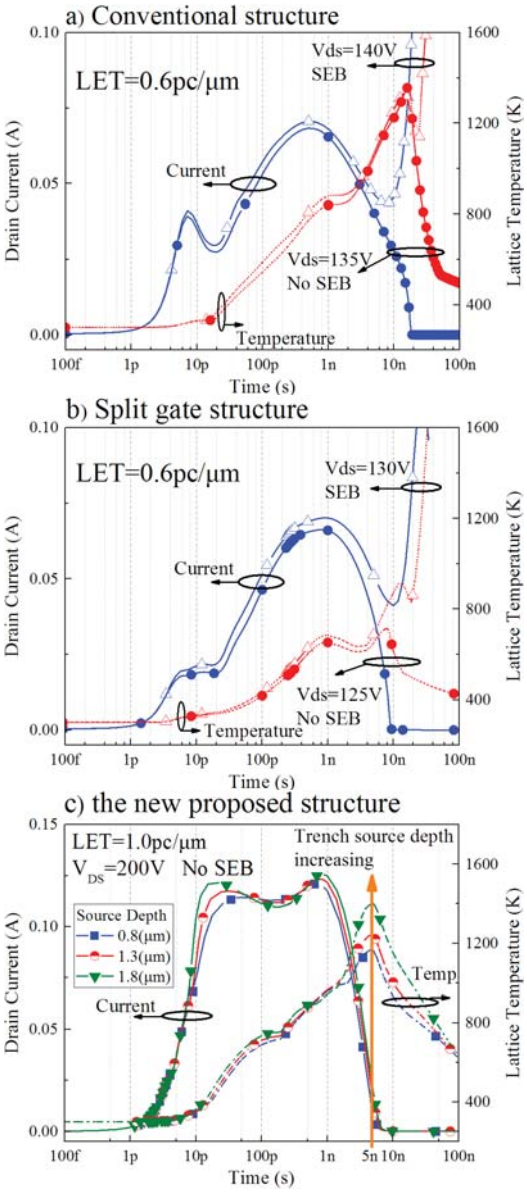

Fig. 3. Simulated SEB response of three structures at the critical value: a) the conventional structure, b) the split structure and c) the new proposed structure.

Fig. 3 shows the extracted SEB threshold voltage and LET value with 3D simulation. For the conventional structure, the SEB occurs under drain voltage 140V and LET value 0.6pC/μm. For the split gate structure, Fig. 3(b)

shows that SEB happens under drain voltage 130V and LET value 0.6pC/μm. It can be seen that the drain current and the lattice temperature increase continually, which is mainly related to the electric-thermal self-sustained phenomenon due to the transient electric field shifting phenomenon (the Kirk effect) and avalanche behavior with local elevated temperature. [10-11]

However, unlike the conventional structure and traditional split gate structure, the new proposed structure demonstrates a superior SEB performance. It can be seen in Fig. 3(c) that the new proposed structure with a trench depth 0.8μm (baseline structure) shows no SEB under the 200V rated breakdown voltage and the LET value of 1pC/μm. According to the conclusion provided in the Ref [9], if the proposed structure shows no SEB under heavier ion species, the device will not exhibit SEB under other lighter ions either. The new proposed structure presents a superior SEB survivability compared with the previous structure.

When the energetic heavy ions travel into the device, huge transient currents are produced inevitability. The parasitic bipolar transistor inherited in the power MOSFET can be triggered if these transient currents pass the sensitive area of the parasitic bipolar transistor. Therefore, many optimization technologies were used to keep the transient current away from the sensitive area (pwell region below the N+ source) as much as possible. In the new structure, the most sensitive area is replaced by the widened gate structure. But if the extensive transient currents (mostly are holes) produced by the high drain bias voltage and the high energy ions become larger and toward around the N+ region, the electric-thermal self-sustained phenomenon still can occur eventually. To improve this situation, the trench source is used to discharge the holes before it arrives the sensitive area of the parasitic bipolar transistor. Therefore, The SEB behavior related to the work of the parasitic bipolar transistor in the new proposed structure can be reduced to a minimum degree, as shown in the Fig. 1(c).

IV. CONCLUSION

A novel trench gate power MOSFET is proposed and analyzed by 3D numerical simulation. This proposed structure is designed by using the partially widened split gate and trench source structure. The fabrication technology of the new structure is compatible with the standard trench power device fabrication process and the structure feature can be used for all voltage ratings device with trench gate structure. Simulation results show that the high blocking ability and a great $R_{DS(ON)}\times Q_{GD}$ FOM characteristics can be achieved compared with the conventional structure. In addition, the new structure shows no SEB under the 200V rated breakdown voltage and the LET value 1pC/μm (approximately the maximum LET value of gold or bismuth ion). Therefore, this proposed structure presents a superior single-event radiation hardness performance without sacrificing other electrical parameters.

ACKNOWLEDGMENT

This work was supported in part by the National Key Research and Development Program of China under Grant No. 2017YFB0400404, in part by the Sichuan Science and Technology Program, and in part by the High Technology Industrialization Special Fund of Cooperation between Province and Academy under Grant 2016SYHZ0026

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