1200 V buried gate fin p-body IGBT with ultralow on-state voltage and good short circuit capability

Jiang Lu✉, Jiawei Liu, Xiaoli Tian, Hong Chen, Yun Bai, Fei Liang and Xinyu Liu

A buried gate fin p-body insulated gate bipolar transistor (BG-Fin-P IGBT) is proposed to achieve ultralow on-state voltage drop ($V_{CE(sat)}$) and good short-circuit (SC) ruggedness simultaneously. A buried gate is introduced at the bottom part of the fin structure, forming a local region with the nanoscale mesa width, which enhances the conductivity modulation effectively. Meanwhile, a relatively wide mesa width (>0.5 μm) can be adopted at the main fin structure to maintain a good SC capability. Compared to the previously reported ultra-narrow-mesas fin p-body IGBT, simulation results reveal that the $V_{CE(sat)}$ of the BG-Fin-P IGBT is reduced from 1.39 to 1.03 V at the current density of 100 A/cm^2 without SC ability degradation. Meanwhile, more than 10 μs short circuit withstand time is enabled at the junction temperature of 423 K for all structures. Moreover, the proposed structure can avoid a fabrication difficulty of the emitter contact when a very narrow mesa width (~30 nm) is required to achieve the ultralow $V_{CE(sat)}$, which brings design freedom on the device's structure.

Introduction: The insulated gate bipolar transistor (IGBT) is an advanced power semiconductor device, which is widely used in medium- and high-power electronic system applications. Many technical innovations have been made in achieving a good trade-off between on-state voltage drop ($V_{CE(sat)}$) and turn-off loss (E_{off}) without sacrificing other device's parameters and reliability. Recently, Feng *et al.* reported an ultra-narrow-mesas fin p-body IGBT (U-Fin-P IGBT) to improve the trade-off relationship effectively, while maintaining other structure advantages [1, 2]. According to the theoretical prediction given by published articles [3, 4], the $V_{CE(sat)}$ can be reduced to close the theoretical limit when the mesa width shrinks to the nanoscale (20–40 nm). However, when the mesa width of the U-Fin-P IGBT reduces <0.5 μm, a severe short-circuit degradation phenomenon occurs due to the collector bias induced barrier lowering (CIBL) effect [1, 5]. Tanaka and Nakagawa explained that the CIBL phenomenon is related to the enhanced conductivity modulation in the channel inversion layer [6, 7]. Although some methods have been given to suppress CIBL behaviour in the very narrow mesa structure by using the deep p+ diffusion layer at the p-body region [7, 8]. However, when the mesa width reduces to the nanoscale, it will bring a great challenge on the fabrication technology of emitter contact, especially for the 20–40 nm width. Moreover, the gate oxide thickness and gate threshold voltage also need to adjust carefully for the IGBT with very small size cells based on the scaling rule design theory [9]. In this Letter, a buried gate fin-P IGBT (BG-Fin-P IGBT) is proposed to reduce the $V_{CE(sat)}$ while maintaining a good short circuit ruggedness and fabrication flexibility.

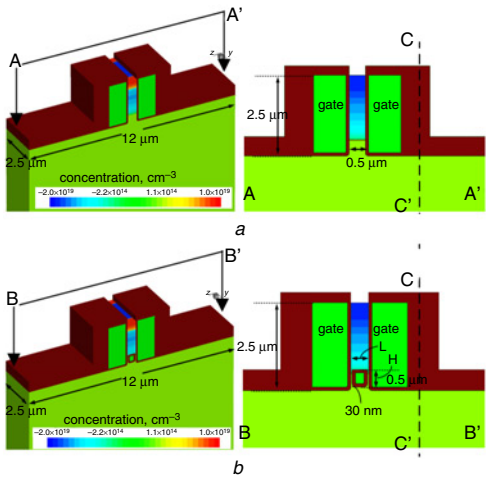

Fig. 1 *Schematic cross-sectional of Fin-P IGBT*

a U-Fin-P IGBT
b Proposed BG-Fin-P IGBT

Device structure and fabrication process design: Fig. 1 shows the cross-sectional view of the U-Fin-P IGBT and the proposed BG-Fin-P IGBT, respectively. Major doping profiles and dimensional parameters are identical for a fair comparison. The detailed structure parameters of the two devices are shown in Table 1. The mesa width of U-Fin-P IGBT remains at 0.5 μm and the mesa width of the BG-Fin-P IGBTs are varied with three sizes (structure A $L = 0.5$ μm; structure B $L = 1$ μm; structure C $L = 2$ μm, as shown in Table 1). In addition, a local 30 nm mesa width region is formed by using a buried gate (BG) structure in all BG-Fin-P IGBT structures. According to the prediction given by Nakagawa [3], the 30 nm mesa width can achieve the lowest $V_{CE(sat)}$ closed to the theoretical limit.

Table 1: Major structural parameters

Structural parameters (unit: μm)	U-Fin-P IGBT	BG-Fin-P IGBT
cell pitch	12	12
N-drift thickness	120	120
N-drift doping, cm^{-3}	1×10^{15}	1×10^{15}
gate oxide thickness	0.1	0.1
silicon trench gate depth	2.5	2.5
silicon mesa width	0.5	A: $L = 0.5$
		B: $L = 1$
		C: $L = 2$
mesa width at BG region	N.A.	0.03
BG height	N.A.	0.5
surface n+/p+ pattern geometry	segment	segment
distance between adjacent n+ segments	2	2
P-body peak doping, cm^{-3}	2.3×10^{17}	2.3×10^{17}

Fig. 2 shows the major front-side process flow to fabricate the BG-Fin-P IGBT structure. First, a trench region is etched and a BG is formed at the N-drift region, as shown in Fig. 2*a*. Note that the polysilicon of the BG structure is connected at the cell edge area for a required gate bias. Obviously, the BG width is slightly smaller than the Fin (mesa) width to form a local very narrow mesa width region. Next, a top silicon material and N-drift region silicon are integrated with room temperature silicon direct bonding (SDB) technology [10] and then the chemical mechanical polishing (CMP) technology is used to achieve a suitable thickness of the p-body, as shown in Fig. 2*b*. After that, the p-body and p+/n+ segments region are formed with implanting technology. Then the wide trenches are etched to form Fin structure, which has been a mature fabrication process for the nanoscale FinFET devices [11–13]. It can be seen in Fig. 2*c* that the local nanoscale mesa width (30 nm in the baseline structure) is created. Finally, the full device structure is formed with the same fabrication process for the Fin-P IGBT, as shown in Fig. 2*d*.

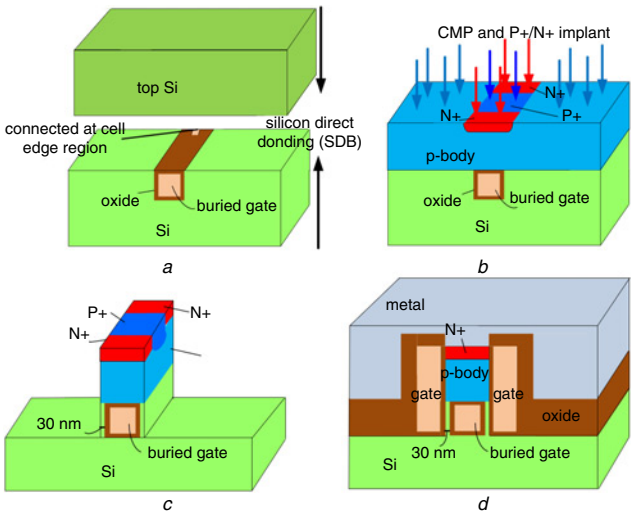

Fig. 2 *Major front-side process flow for BG-Fin-P IGBT*

a Formation of BG structure and SDB technology
b CMP technology and formation of p-body, n+ and p+ regions
c Etching for Fin structure
d Formation of final structure

Simulation results and discussion: All simulated structures are investigated by using Sentaurus 3D TCAD simulation software from Synopsys. For comparison purpose, all structures are designed based on 1.2 kV U-Fin-P IGBT and the major structure are calibrated against the simulated results in [1]. The major physical models for silicon IGBT structure are employed. Fig. 3*a* shows the simulated blocking ability. It can be seen that the breakdown voltages of all structures are over 1.3 kV. The on-state hole carriers distribution along the vertical line CC′ in the N-drift region (as shown in Fig. 1) is given in Fig. 3*b*. At the same backside collector doping concentration, the hole carrier distribution of the proposed structures shows almost one order of magnitude higher than that of the U-Fin-P IGBT. In the on-state, the huge hole carriers are blocked at the BG region due to the local nanoscale mesa width, resulting in an effectively enhanced conductivity modulation. Therefore, the BG-Fin-P IGBT can achieve an ultralow $V_{CE(sat)}$.

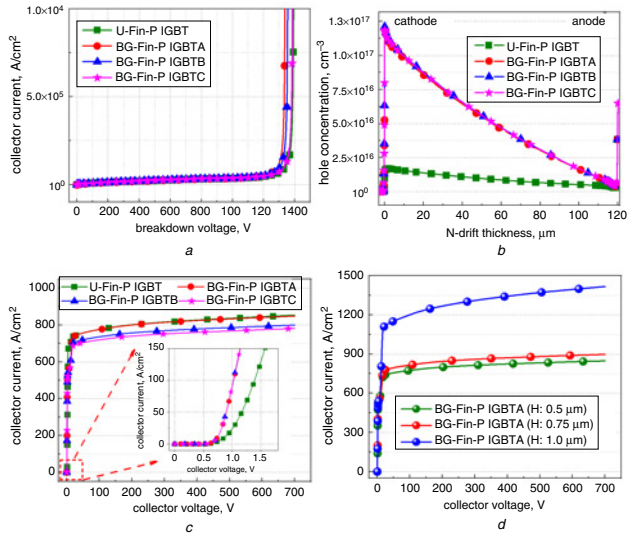

Fig. 3 *Simulated characteristics comparison of U-Fin-P IGBT and proposed BG-Fin-P IGBT*

a Breakdown voltage curves
b On-state hole carrier distribution along vertical line CC′
c Forward *I–V* curves
d Forward *I–V* characteristics of BG-Fin-P IGBT with different BG heights

Fig. 3*c* shows the forward *I–V* characteristics of all structures. At the current density of 100 A/cm^2, a gate bias $V_{ge} = 15$ V and the same backside dose concentration, the $V_{CE(sat)}$ of the BG-Fin-P IGBTs (1.03 V) is 26% lower than that of the U-Fin-P IGBT (1.39 V). In addition, it can be seen that the saturation current of the proposed structures is similar to that of the U-Fin-P IGBT. Note that much wider mesa width can provide a slightly lower saturation current due to the reduced channel current density. Most importantly, the saturation current degradation phenomenon is not observed in all proposed structures. In addition, the proposed structure avoids the manufacturing difficulty of emitter contact at a very narrow mesa width situation, which provides an extra degree of freedom in the structure design.

To investigate the influence of the BG further, the BG height is analysed by varying the *H* value from 0.5 to 1 μm. According to the simulation results given in Fig. 3*d*, it can be known that the saturation current increases as the rising of the BG height *H*. The main reason is that the effective space for the depletion layer extension becomes smaller as the increase of the height *H*, which influences the channel pinch-off behaviour. Therefore, the BG height 0.5 μm is an optimised selection in our simulation structure.

Fig. 4 shows the short circuit characteristics for all structures. The DC bias voltage is 800 V, the stray inductance is 50 nH and the gate resistor is fixed at 30 Ω. The short circuit behaviour is investigated by using the mixed electro-thermal simulation at 423 K atmosphere temperature with the thermal resistance 0.01 k/kW·cm^2. It can be seen that the proposed structure presents more than 10 μs short circuit withstands time capability. Obviously, the CIBL behaviour is avoided in the BG-Fin-P IGBT due to the relatively wide mesa width at the main p-body region.

Fig. 5 shows the trade-off of $V_{CE(sat)}$ and E_{off} by varying the backside p+ collector dosages. Simulation results indicate that a better trade-off performance can be provided by the BG-Fin-P IGBT. It can be seen that at the same E_{off} value, the $V_{CE(sat)}$ of the BG-Fin-P IGBT is 14% lower than that of the U-Fin-P IGBT. Meanwhile, the BG-Fin-P IGBT with 20 nm local mesa width shows a similar trade-off with the 30 nm structure due to the saturation phenomenon in the very narrow mesa region [3]. Therefore, the BG-Fin-P IGBT with 30 nm local mesa width is an optimised structure selection.

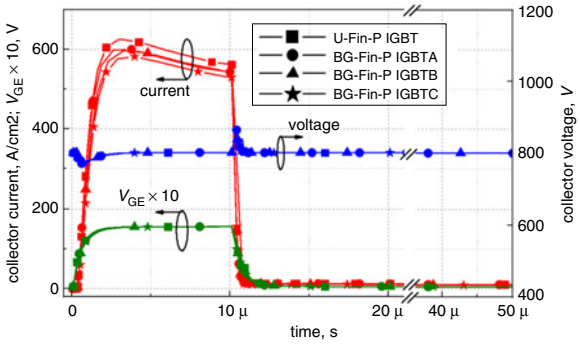

Fig. 4 *Simulated short circuit characteristic of U-Fin-P IGBT and BG-Fin-P IGBTs with different mesa width*

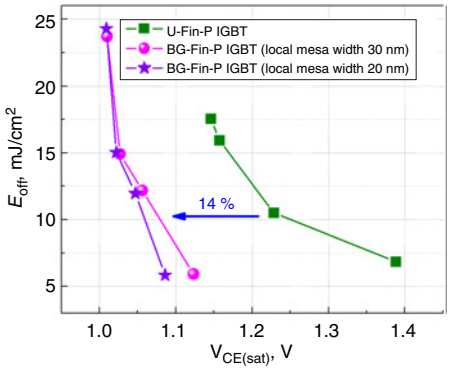

Fig. 5 *Simulated $V_{CE(sat)}$–E_{off} trade-off of U-Fin-P IGBT and BG-Fin-P IGBT*

Conclusion: In this Letter, we present a Fin-P IGBT with BG to enhance conductivity modulation without sacrificing short circuit capability. Simulation results indicate that the $V_{CE(sat)}$ of BG-Fin-P IGBT (1.03 V) can be 26% lower than that of the U-Fin-P IGBT structure (1.39 V) at the same current density. In the on-state, the hole carriers are blocked at the local nanoscale mesa width region owing to the bottom BG structure. Meanwhile, the short circuit degradation phenomenon due to the CIBL effect in the very narrow mesa IGBT is avoided because the main p-body structure can be designed with a relatively wide mesa width. It also brings design freedom of mesa width for the Fin-P IGBT without the fabrication difficulty of the emitter contact.

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