Description

The CV8013NK is a high efficiency, Qi-compliant wireless power receiver, targeted for 5W portable applications. The CV8013NK converts an AC power signal from a resonant tank into a regulated DC output voltage with 5V. Which integrated Low RDS(on) synchronous rectifier and ultra-low dropout offer high efficiency making the product ideally suited for battery-operated applications.

CV8013NK integrated an 1T-8051 Microprocessor offering a high level of program ability, an 12bit high precise ADC, a programmable current limit. High integration, To minimizing the external component count and cost effective solution. Work with different WPC compliance transmitter (TX), CV 8013 can deliver 5W.

Wireless power system

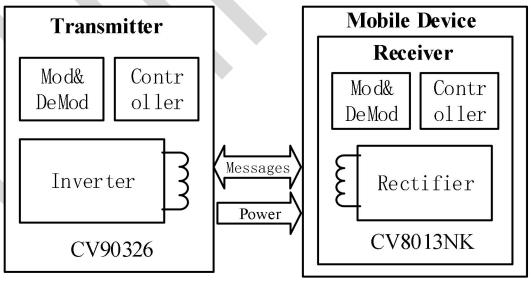


Figure 1 CVS Wireless Power System

Features

- Single-chip RX solution supporting up to 5W application
- Compatible with WPC v1.2.4 Qi Standard
- Internal Integrated High efficiency Synchronous Rectifier
- Up to 83% peak DC-DC efficiency with CV90326 TX
- Programmable current limit
- Embedded Microprocessor
- Over voltage, over current, over temperature protection
- Integrated AD-Enable for wireless by-pass
- ~20 to +85°C ambient operating temperature range
- QFN32 (5mm x 5mm; 0.5mm pitch)

Typical Applications

- Wireless power RTx solution for portable devices
- Mobile phone
- TWS Earbuds
- E-cigarettes
- Tablets
- Accessories
- Stationary device power supply

1. Block diagram

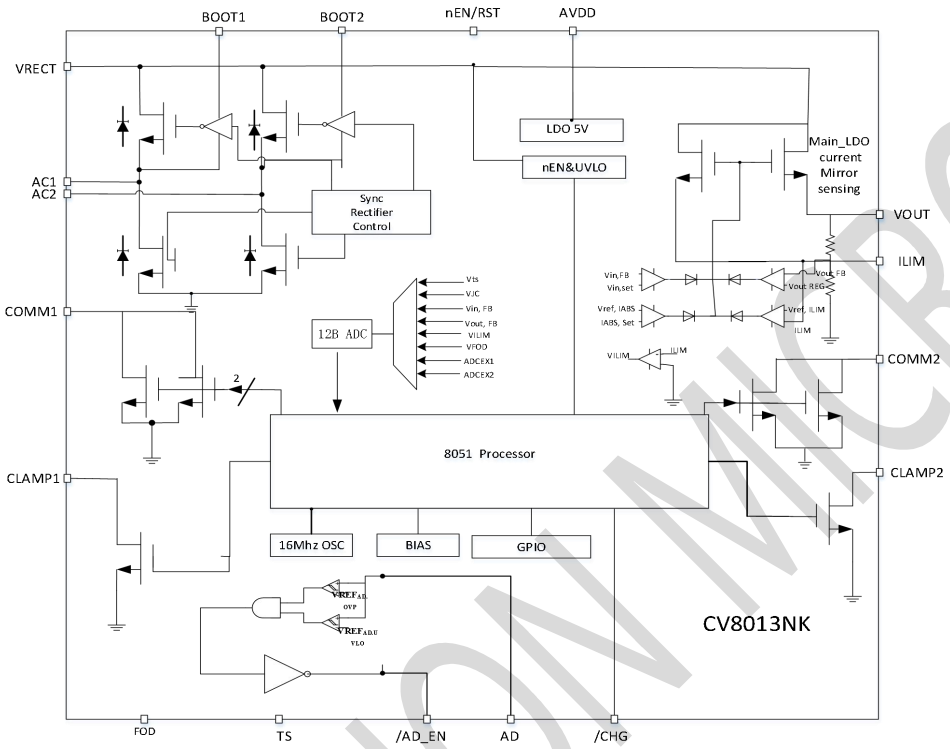


Figure 2 Block diagram of CV8013NK

1.1 Typical Application Circuit

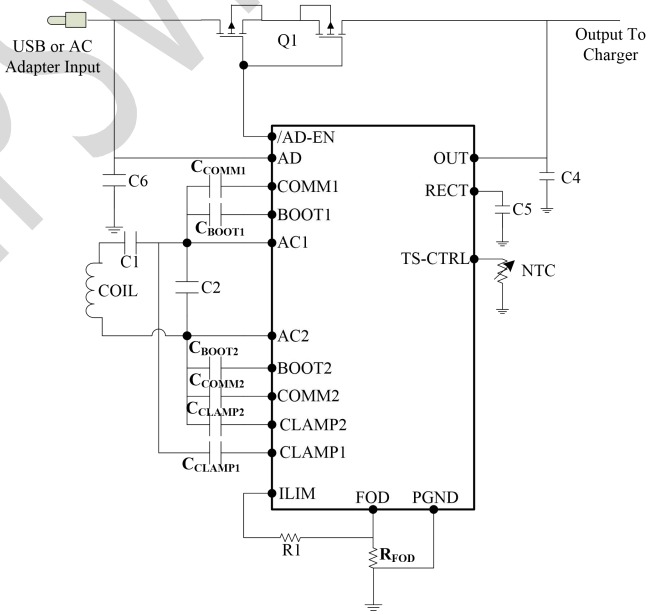


Figure 3 Typical application schematic of CV8013NK

2. Pin Assignments

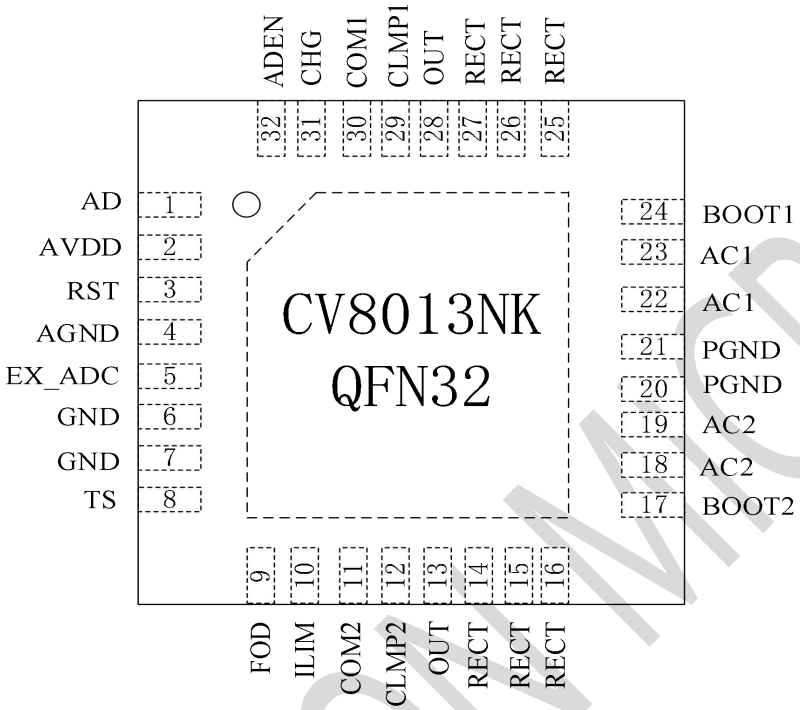


Figure 4 Bottom View

2.1 Pin configuration and functions

PIN NO	PIN NAME	I/O	DESCRIPTION
1	AD	I	Adapter sense pin.
2	AVDD	P	Supply voltage
3	RST	I	Chip disable, Pull High voltage to stop wireless charging
4	AGND	P	Ground
5	EX_ADC	I	Minimum voltage configuration
6	GND	P	Ground
7	GND	P	Ground
8	TS	I	Temperature sense, connect to NTC thermistor resistor
9	FOD	I	Input pin to use for FOD calibration
10	ILIM	I/O	Programmable over-current limit pin. Connect to over-current protection resistor
11	COM2	O	Open drain output used to communication with TX coil by varying reflected impedance. Connect through a capacitor to either AC2 for capacitive load modulation.

PIN NO	PIN NAME	I/O	DESCRIPTION
12	CLMP2	O	When the Vrect voltage goes bove 15v, To connect on capacitance (or Resistor) to reduce coupling for device protection.
13	OUT	O	Output pin, used to deliver power to the load
14	RECT	O	Filter capacitor for synchronous rectifier .
15	RECT	O	Filter capacitor for synchronous rectifier .
16	RECT	O	Filter capacitor for synchronous rectifier
17	BOOT2	O	Bootstrap capacitors for driving the high side FETs of the synchronous rectifier. Connect a 10nF capacitor from BOOT2 to AC2.
18	AC2	I	AC input power via external coil
19	AC2	I	AC input power via external coil
20	PGND	P	Ground
21	PGND	P	Ground
22	AC1	I	AC input from receiver coil
23	AC1	I	AC input from receiver coil
24	BOOT1	O	Bootstrap capacitors for driving the high side FETs of the synchronous rectifier. Connect a 10nF capacitor from BOOT1 to AC1
25	RECT	O	Filter capacitor for synchronous rectifier
26	RECT	O	Filter capacitor for synchronous rectifier
27	RECT	O	Filter capacitor for synchronous rectifier
28	OUT	O	Power output, used to deliver power to the load
29	CLMP1	O	When the Vrect voltage goes bove 15v, To connect on capacitance (or Resistor) to reduce coupling for device protection.
30	COM1	O	Open drain output used to communication with TX coil by varying reflected impedance. Connect through a capacitor to either AC1 for capacitive load modulation.
31	/CHG	O	Charging indicator.
32	/AD_EN	O	Push-pull driver for dual PFET circuit that can pass AD input to the OUT pin; Used for adapter MUX control.

3. Electrical characteristics

3.1 Absolute Maximum Rating

Parameter	Condition	MIN	TYP	MAX	UNIT
Input Voltage	CHG,FOD,TS,ILIM,OUT	-0.3		7	V
	Other Pins	-0.3		20	V
Input Current	AC1, AC2			2	A(RMS)
Output Current	OUT			1.25	A
Junction Temperature				150	ºC
ESD(HBM)	All pins			2	kV

3.2 Thermal characteristics

Parameter	Description	MIN	TYP	MAX	UNIT
Θ_{JA}	Junction to ambient thermal resistance		47		ºC/W

3.3 Recommend characteristics

Parameter	Description	MIN	TYP	MAX	UNIT
RCET	Input voltage range			12	V
I_{IN}	Input current			1.5	A
I_{OUT}	Output current			1	A
I_{COMM}	COMM current			0.5	A
T_J	Junction Temperature	0		125	ºC

3.4 Electrical characteristics

Parameter	Description	MIN	TYP	MAX	UNIT
UVLO	Under-voltage lock out		5	5.1	V
$V_{RECT(OVP)}$	V_{RECT} over voltage protection		12		V
$V_{RECT(REG)}$	V_{RECT} range set by communication	V_{OUT}+0.12		V_{OUT}+2.0	V
$V_{OUT(REG)}$	Regulated output voltage		5.0		V
I_{OUT}	Output current range		1		A
V_{TS}	Temperature sense bias voltage	4.5	5.0	5.5	V
R_{TS}	Pull-up resistor for TS to bias voltage	90	100	110	kΩ
$T_{J(SHUTDOWN)}$	Thermal shutdown temperature		150		ºC
$T_{J(HYS)}$	Thermal shutdown hysteresis		20		ºC
$R_{DS(ON,COM)}$	COM1 and COM2		1.0		Ω
f_{COMM}	Communication frequency		2.0		kb/s
$R_{DS(ON,CLAMP)}$	CLAMP pin MOSFET		0.5		Ω

4. Function description

4.1 Sync Rectifier

Dynamic rectifier adjust the purpose is to optimize efficiency and reduce the overall LDO power consumption

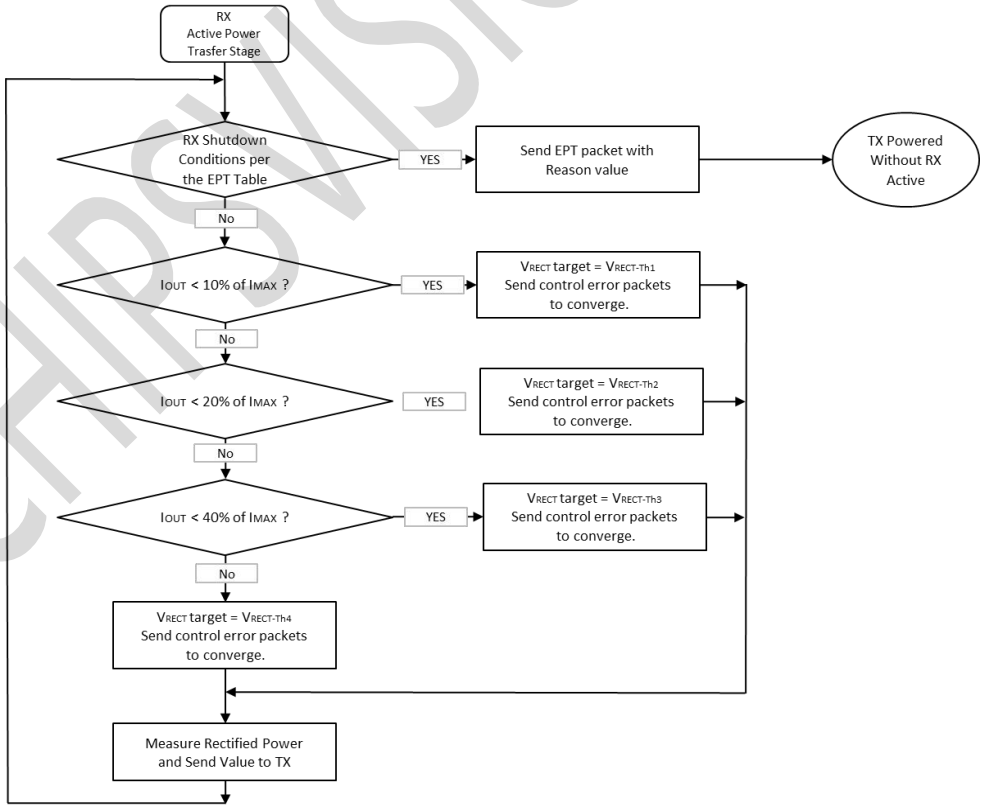
$$P_{DIS} = (V_{RECT} - V_{OUT})*I_{OUT}$$

The rage of dynamic adjustment is as follows (see table below)

Output Current Percentage	V_{RECT} (V)
0~10%	V_{OUT} + 2.00
10%~20%	V_{OUT} + 1.5
20%~40%	V_{OUT} + 0.56
>40%	V_{OUT} + 0.12

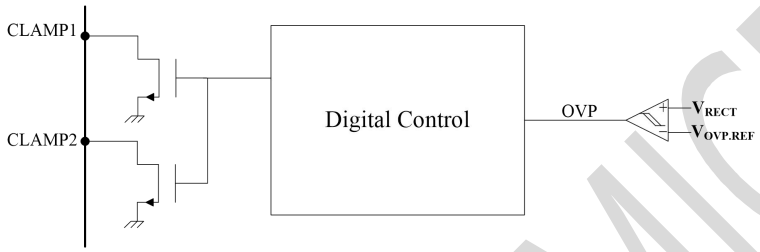
Wherein, I_{OUT} current percentage is determined according to the maximum output current I_{MAX} setting by R_{ILIM}.

V_{RECT} Dynamic adjustment is accomplished by the controlling program of RXthrough communicating with TX. Control flow chart is as below.



4.2 VRECT Over-voltage protection

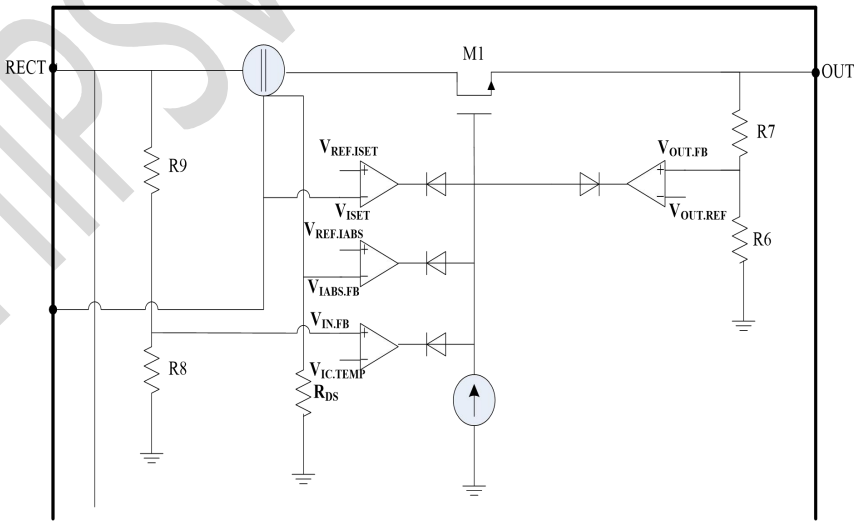
VRECT through internal comparator, generate over-voltage signal OVP and send the OVP signal to digital logic. Digital logic sends OVP interrupts to MCU. RX controlling program drives CLMP pin to cause RX coil to be detuned to reduce the amount of the received energy. Thereby, rapidly reduce VRECT to a safe range.



4.3 VRECT relevant parameters

Parameter	Description	MIN	TYP	MAX	UNIT
$V_{RECT(REG)}$	V_{RECT} range set by COMM	V_{OUT}+0.12		V_{OUT}+2.0	V
$V_{RECT(TRACK)}$	V_{RECT} above V_{OUT}		120		mV
$V_{OVP,REF}$	V_{RECT} over voltage protection		12		V
$R_{DS(ON)}$	CLAMP pin MOSFET		0.5		Ω

4.4 LDO



LDO schematic diagram is as above. The functions of the 4 amplifiers are as follows.

4.5 VOUT, FB

V_{OUT} is fed back to the amplifier negative input through a resistor divider network and compare with the internal default setting to control M1 to output the stable voltage.

The relevant parameters are as follows：

Parameter	Description	MIN	TYP	MAX	UNIT
K_{RO}	Feedback Resistor Ratio	1.2/8.0		1.2/4.5	
$V_{OUT,REG}$	V_{OUT} Reference		1.2174		V
$I_{OUT,\ MAX}$	Max Current Limit			1..25	A
$I_{OUT,\ DIS}$	Quiescent Current when disabled		20	35	μA

4.6 VILIM

The R_{ILIM} , is the external resistor connected with ILIM pin. The voltage sampling value V_{ILIM} input to the amplifier negative input pin and is compared with the reference voltage $V_{ILIM,REF}$. If the voltage value V_{ILIM} exceeds the threshold $V_{ILIM,REF}$, then reduce I_{OUT} output current by controlling M1.

The calculation of maximum output current I_{MAX} is as follows：

$$R_{ILIM}=K_{ILIM}/I_{MAX}$$

Considering 20% margin of the setting value I_{MAX}, $I_{ILIM}=1.2*I_{MAX}$ .R_{ILIM} is calculated by the following equation.

$$R_{ILIM}=K_{ILIM}/I_{LIM}= K_{ILIM}/1.2I_{MAX}$$

The relevant parameters are as follows：

Parameter	Description	MIN	TYP	MAX	UNIT
K_{ILIM}	Current Limit Factor		450		Ω
$V_{ILIM,REF}$	I_{LIM} Reference		1.2		V

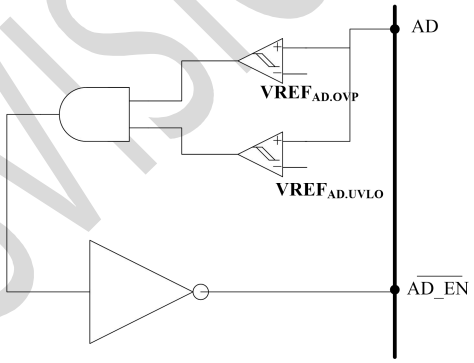
4.7 End Power Transfer Package (WPC Header 0x02)

The WPC allows for special commands for the receiver to terminate power transfer from the

transmitter termed End Power Transfer (EPT) packet. The table below specifies the V1.2 reasons column and their corresponding data field value. The condition column corresponds to the methodology used by CV8013NK to send equivalent message.

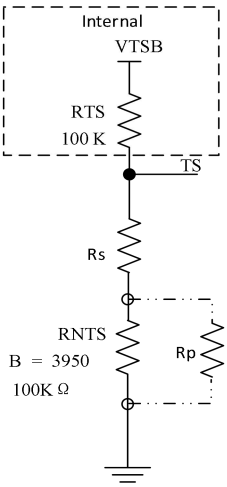
MESSAGE	VALUE	CONDITION
Unknown	0x00	AD>3.6V
Charge complete	0X01	TS/CTRL <0.3V; charge complete
Internal Fault	0x02	Vic,TEMP: Vic_TEMP>Vj,Off
Over temperature	0x03	TS < VHOT
Over voltage	0x04	NOT Send, Send 0x03 code to reduce power transfer in this case.
Over current	0x05	Not Send
Battery Failure	0x06	Not Send
Reconfigure	0x07	Not Send
No Response	0x08	Once Vrect voltage cannot reach 6.5V

4.8 Adapter Enable



In order to be compatible with external adapter plugged in, AD pins are used to monitor the input voltage of adapter. When AD is above $VREF_{AD,OVP}$, means external adapter is plugged in. Internal comparatorpulls AD_EN pin to logic low. AD_EN at logic low drives external PMOS to enable the wired charging path. Meanwhile, AD_EN signal is sent to digital logic, RX control program sends EPT to notify TX to stop power transmission. If AD_EN is below $VREF_{AD,OUVLO,}$ means external adapter is unplugged. Internal cooperator pulls AD_EN pin to logic high, cut off the wired charging path and the chip.

4.9 External Temperature Sense



TS pin is used to monitor the external temperature by using NTC resistor network. Internal pull-up resistor V_{TSB} RTS and external resistor composes voltage division circuit. The internal ADC converts the value of V_{TS} voltage. And the over temperature protection will be triggered when the V_{TS} less then 1V. the RX will send EPT （end power transfer） package to TX, and stop to output.

*To revise Rs and Rp resistors to change over temperature protection (OTP) trigger point setting,

Rs=0Ω， Rp: NC， the OTP trigger point is 60° C；

The calculation formula is as follow:

(5V*Rntc)/(RTS+Rntc)=1V

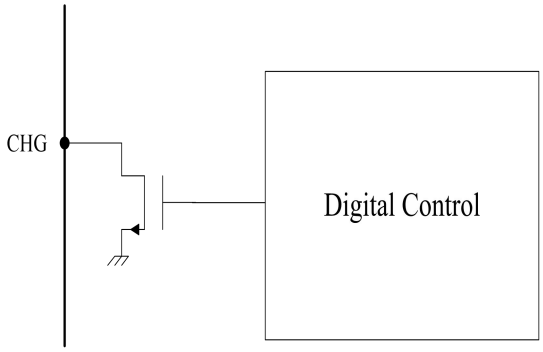
To rise Rs resistance value, the OTP trigger point will be rised (>60° C);

To select resistor value for Rp to set OTP triggle point (<60° C);

The related parameters are as follows：

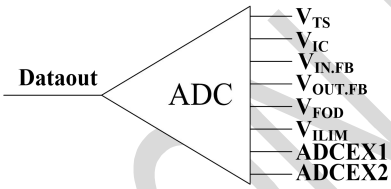
Parameter	Description	MIN	TYP	MAX	UNIT
V_{TSB}	Internal TS Bias Voltage		5		V
R_{TS}	Pullup Resistor for NTC		100		kΩ

4.10 Charging Status



Digital logic drives CHG pin to notify external system that I_{OUT} is being output, indicating that wireless charging is in progress.

4.11 Internal ADC



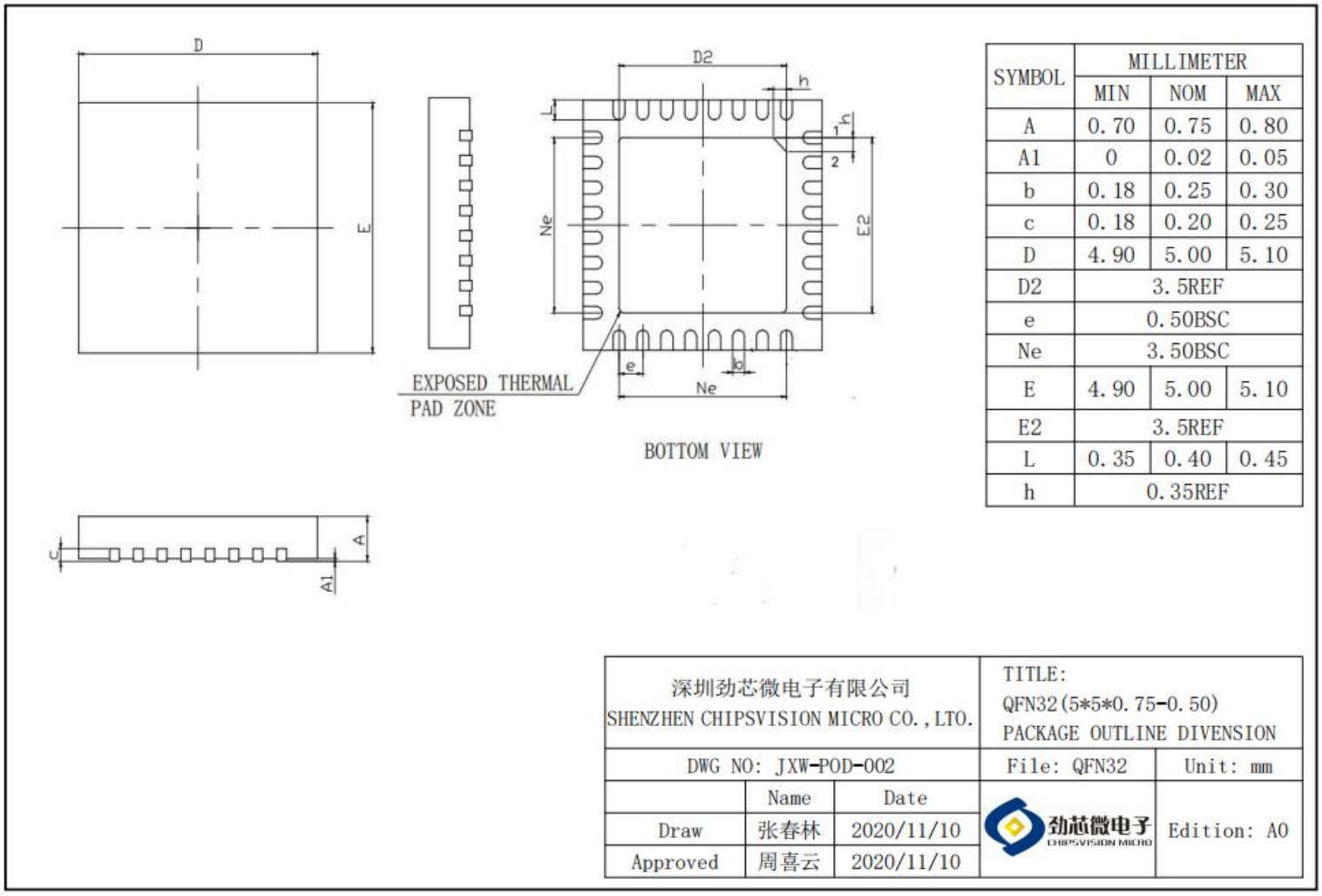
ADC input 8 sets internal voltage signals and sends to digital logic after digital-to-analog conversion. RX control program make the corresponding detection and judgment.

Input Signal	Description	Range (V)
V_{TS}	External Temperature Sense Voltage	TBD
$V_{IC,TEMP}$	Internal Temperature Sense Voltage	TBD
$V_{IN,FB}$	V_{RECT} Feedback Voltage	TBD
$V_{OUT,FB}$	V_{OUT} Feedback Voltage	TBD
V_{FOD}	I_{OUT} sample Voltage	TBD
V_{ILIM}	I_{LIM} sample Voltage	TBD
ADCEX1	External Analog Signal1	TBD
ADCEX2	External Analog Signal2	TBD

5. Package information

Orderable Part Number	Description and Package	MSL Rating	Shipping Packaging	Ambient Temperature
CV8013NK	QFN32 (5mm x 5mm; 0.5mm pitch)	MSL3	Tape and reel	0°C to +85°C

Note:The package outline drawings is on page 14 of this document.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.5REF		
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.5REF		
L	0.35	0.40	0.45
h	0.35REF		

深圳劲芯微电子有限公司 SHENZHEN CHIPSVISION MICRO CO.,LTO.			TITLE: QFN32(5*5*0.75-0.50) PACKAGE OUTLINE DIVENSION	
DWG NO: JXW-POD-002			File: QFN32	Unit: mm
	Name	Date	劲芯微电子 CHIPSVISION MICRO	Edition: A0
Draw	张春林	2020/11/10		
Approved	周喜云	2020/11/10		

6. Typical Application Schematics