High-efficiency, High-power Wireless Charging Transmitter SoC

Overview

CV90362A is a wireless charging transmitter system-on-chip (SoC), which supports various types of power supply adapters such as PD2.0, PD3.0, QC2.0, QC3.0, and AFC. CV90362A supports the latest Qi V1.2 and Qi V1.3 versions, single-coil/multi-coil wireless charging applications, diversified charging specifications such as BPP 5W, Apple 7.5W, Samsung 10W, and EPP 15W, as well as private agreements of customers in line with Qi standard, with a power of up to 100 W.

CV90362A provides a variety of functions, including under-voltage protection, hardware over-voltage protection, over-current protection, and over-temperature protection. It also supports Q value and FOD detection.

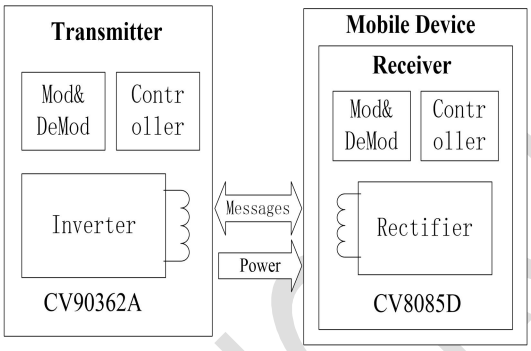
Integrated with the full-bridge driver circuit as well as voltage and current communication decoding function modules, CV90362A adopts QFN48 package to significantly reduce PCB size and save BOM cost.

Application

☆ Standard, high-power wireless charging base

☆ On-board wireless charging device

☆ Mobile power wireless charging device



Features

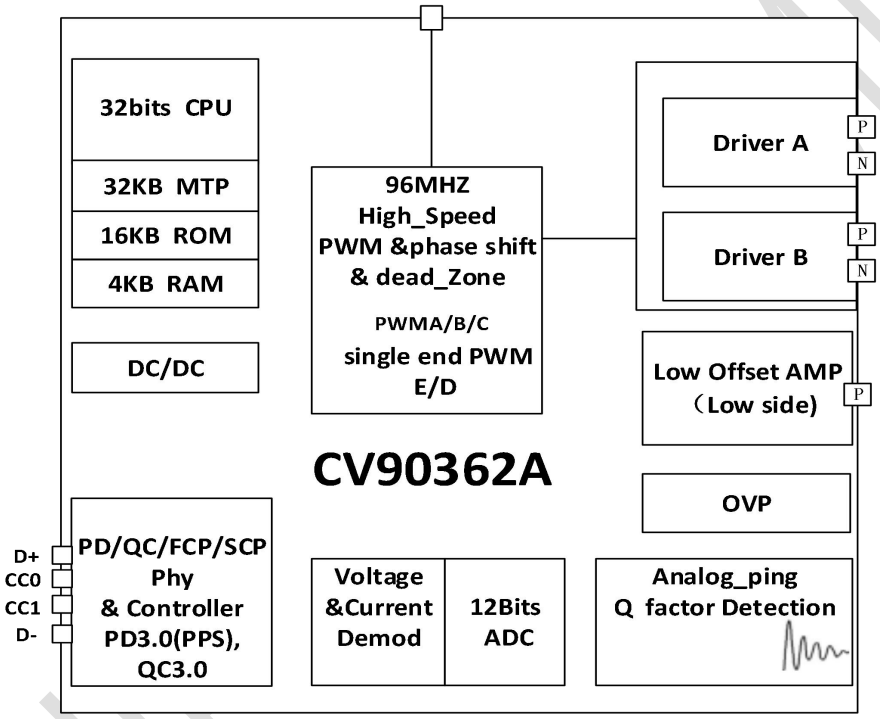
- In compliance with Qi V1.2 and Qi V1.3 standards;
- Support for diversified charging specifications such as BPP 5W, Apple 7.5W, Samsung 10W, and EPP 15W, as well as private agreements of customers in line with Qi standard, with a power of up to 100 W;
- Wireless charging for up to 2 Rx devices simultaneously;
- Built-in 32-bit high-speed CPU core;
- Built-in 32 KB MTP, 16 KB Mask ROM, 4 KB RAM; Type-C port for FW upgrade;
- Support for multiple fast charging protocols such as PD2.0, PD3.0 PPS, QC2.0, QC3.0, AFC and SCP;
- Built-in full-bridge MOS gate driver;
- Four pairs of built-in complementary 16-bit high-speed PWMs at 96 MHz, and two high-speed independent 16-bit PWMs;
- 8-channel 12-bit high-precision ADCs;

- Built-in voltage and dual-channel current decoding;
- Built-in low zero drift operational amplifier;
- Built-in hardware over-voltage protection;
- Support for Q value detection;
- Support for FOD debris detection;
- 11 GPIOs, I2C and UART communication.

Product information

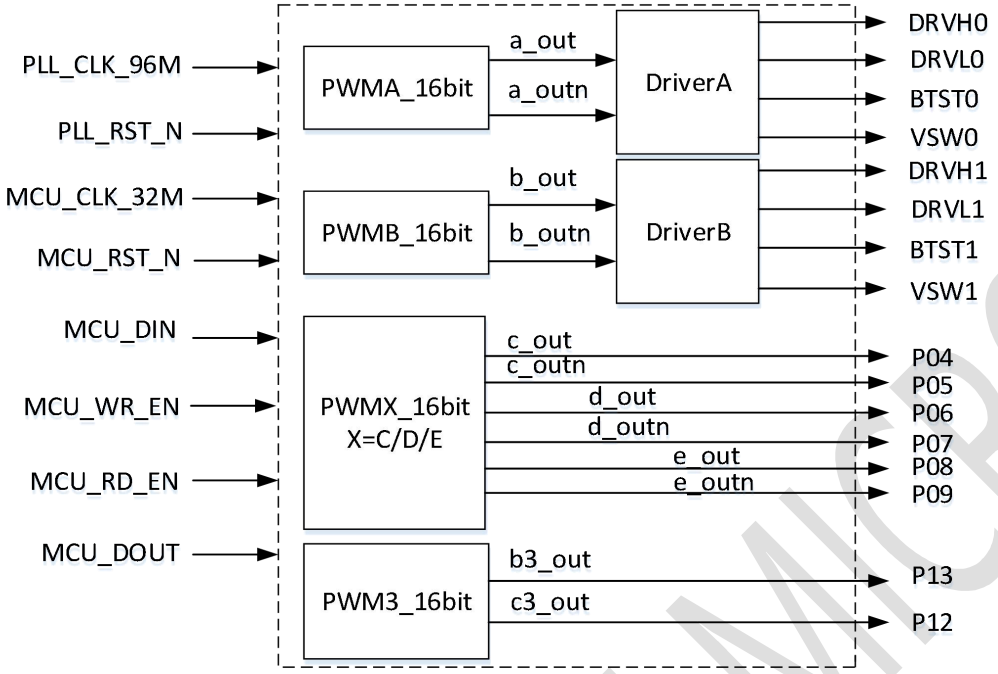
Model	Package	Dimensions
CV90362A	QFN48	6.00 mm × 6.00 mm × 0.75 mm

1. System Drawings



2. Function Description

2.1 Full-Bridge PWM Controller



The PWM is designed with a frequency of 96 MHz and integrated with 5 channels of PWM output, which are A/B, C/D, and E (this article uses i to stand for A/B/C/D/E).

Among them, the complementary output of A, B, and C is i_OUT/i_OUTN, D, and E single-ended output. A and B outputs integrate internal Driver A and Driver B.

Features:

- Each output of A/B, C/D, and E has a 16-bit upward auto-loading counter with a 16-bit configurable period/duty cycle and 8-bit dead zone register;
- It is allowed to update the timer register to repeat the count after a specified number of counter cycles;
- A/B, A/C, and C/D outputs can be combined into a full bridge respectively. Three full-bridge outputs do not interfere with each other. Each group keeps synchronization and supports shift phase, pulse width adjustment, and dead zone. The A/C output can also be combined into a full bridge;
  - A and B outputs form a full bridge, and both share the period and duty cycle of A and use their own dead zones.

    B is based on A and supports phase shift;
  - A and C outputs form a full bridge, and both share the period and duty cycle of A and use their own dead zones.

    C is based on A and supports phase shift. The resources used by C is those of B. The resources of C can be reused by D and work independently;

- C and D outputs form a full bridge, and both share the period and duty cycle of C and use their own dead zones.

  D is based on C and supports phase shift.

- A, B, and C can form 6 PWM complementary outputs.
  - They share the A_COUNT and period of A;
  - They use own duty cycles and dead zones;
  - The resources of C are used by D;
- Brake input supports hardware brake and software brake;
- Each i_OUT/i_OUTN has its own output enable control;
- Support online dynamic change of period, duty cycle, dead zone and 360-degree phase shift register to ensure the integrity of the period;

PWM3_16BIT is composed of two independent PWM outputs, namely, B3_OUT and C3_OUT.

PWM3_16BIT is composed of a 16-bit A_COUNT auto-loading counter.

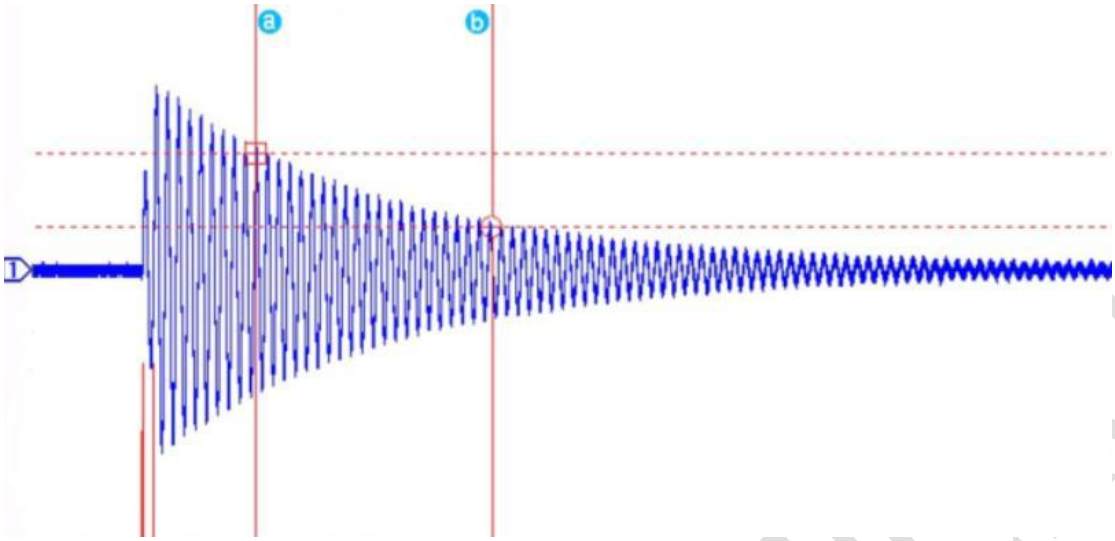
Features:

- Basic timing function;
- Driving 2 PWM waveform outputs at the same time.

2.2 Q Value Detection

Turn on the upper tube of the half-bridge driver to make the LC circuit store a certain amount of energy. Then, turn on the lower tube of the half-bridge driver to make the LC circuit self-oscillate and discharge to form a high-frequency exponentially attenuated oscillation.

The following figure shows the waveform.



Detect the peak voltages of Va and Vb, and record the number of intermediate pulses (N) to calculate the Q value of the circuit using the following formula:

$Q = (2\pi f)\cdot L/R = (Nb-Na)\cdot\pi/\ln(Va/Vb)$;

Va=1000 mV,

Vb=200 mV;

Ln (Va/Vb)=Ln5=1.609.

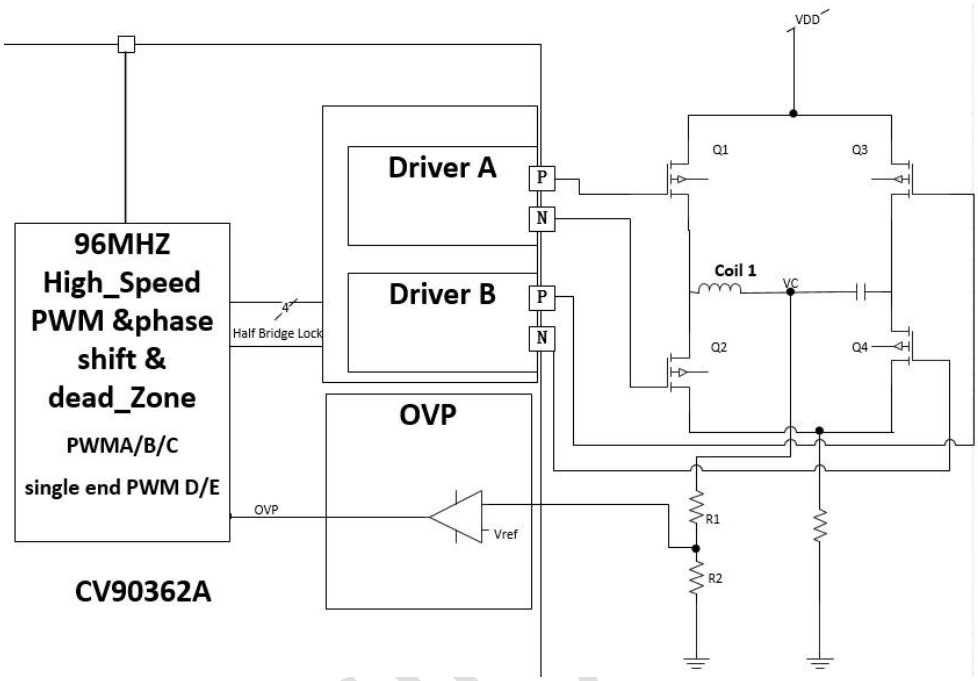
2.3 Ping Simulation

When the CV90362A sends a very short pulse to the LC, and the LC will oscillate. When there is an Rx device approaching, the oscillation amplitude of the LC will change, so that the Rx device is detected. Ping simulation can greatly decrease the average power consumption of Tx device in standby state.

2.4 Hardware Over-voltage Protection

The CV90362A has a built-in hardware over-voltage protection circuit. This circuit enables the chip to have a rapid protection trigger mechanism to avoid high voltage impact on the transmitter system components and receiver equipment due to anomalies (such as debris), which can cause the coil resonance voltage to be ultra high. The CV90362A has a triple over-voltage protection mechanism. The first stage is software protection. When the VC voltage reaches or approaches the protection voltage preset by the software, the software stops increasing the transmitting energy. When the VC voltage exceeds the R1/R2 divided voltage and is higher than the N-end voltage (3.3 V) of the comparator, the second-stage hardware protection mechanism is triggered, and the OVP will generate the Half Bridge Lock signal, which locks the full-bridge driver working mode to half-bridge mode (Q3 is off and Q4 is normally on). At this time, the transmitting energy of the Tx device is halved, and the OVP interrupt is generated. If the Tx device normally receives the communication signal

from the Rx device, the VC voltage does not continue to rise, and the software determines whether the system resumes normal charging. If the VC voltage continues to rise in the half-bridge working mode, the system will trigger the third-stage protection, turn off Q1 and Q3, and normally open Q2 and Q4. The MOSFET enters the discharge state.



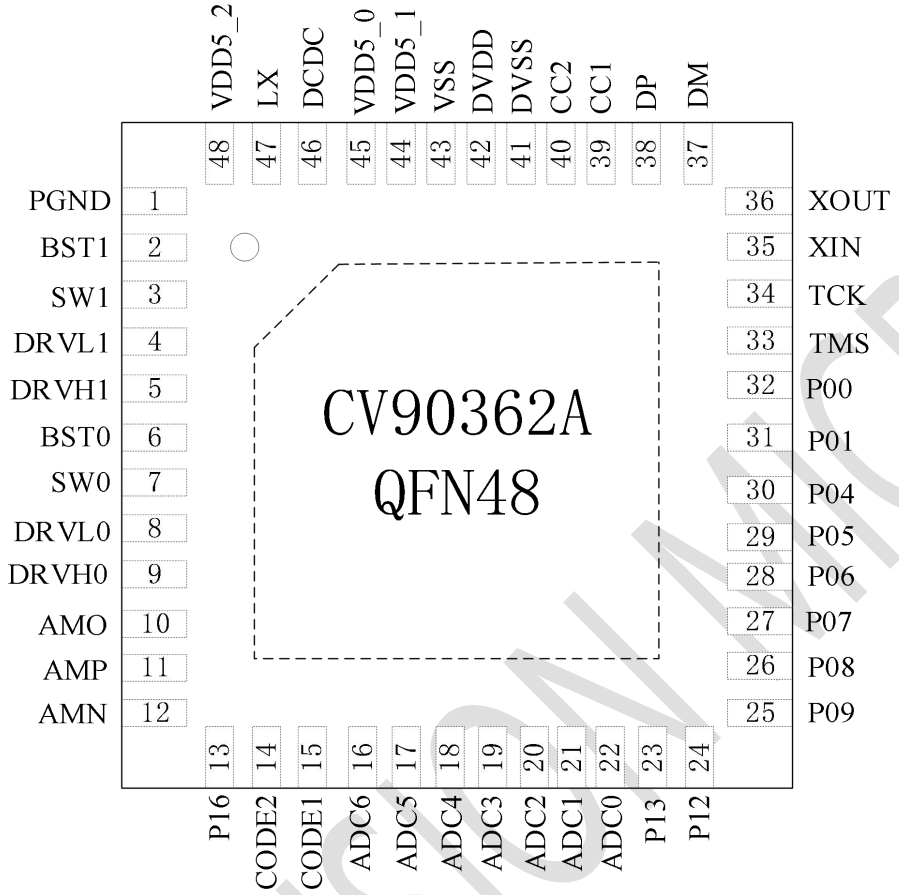
Block diagram of hardware protection circuit

2.5 Debris Detection

The CV90362A uses the Q value detection and power loss methods to detect debris, so as to make accurate and rapid judgment and protection:

- Q value detection: When the Q value detected by the Tx device is lower than the preset value, FOD alarm is generated quickly;
- Power loss: The CV90362A is equipped with a high-precision ADC. When the difference between the transmitting power of the Tx device and the receiving power of the Rx device is greater than the set value, the Tx device will make accurate judgments and implement FOD protection.

3. Pin Definition



3.1 Pin Description

Pin No.	Pin Name	Description
1	PGND	GND
2	BST1	Half-bridge high-voltage driver bootstrap power supply pin 1
3	SW1	Half-bridge high-voltage driver SW connection pin 1
4	DRVL1	Half-bridge low-voltage driver output pin 1
5	DRVH1	Half-bridge high-voltage driver output pin 1
6	BST0	Half-bridge high-voltage driver bootstrap power supply pin 0
7	SW0	Half-bridge high-voltage driver SW connection pin 0
8	DRVL0	Half-bridge low-voltage driver output pin 0
9	DRVH0	Half-bridge high-voltage driver output pin 0
Pin No.	**Pin Name**	**Description**
10	AMO	Operational amplifier output pin
11	AMP	Operational amplifier positive input pin
12	AMN	Operational amplifier negative input pin
13	P16	General digital I/O pin ADC channel input
14	CODE2	Current decoding signal
15	CODE1	Voltage decoding signal
16	ADC6	ADC input channel 6
17	ADC5	ADC input channel 5
18	ADC4	ADC input channel 4
19	ADC3	ADC input channel 3
20	ADC2	ADC input channel 2
21	ADC1	ADC input channel 1
22	ADC0	ADC input channel 0
23	P13	General digital I/O pin
24	P12	General digital I/O pin
25	P09	General digital I/O pin

26	P08	General digital I/O pin
27	P07	General digital I/O pin
28	P06	General digital I/O pin
29	P05	General digital I/O pin
30	P04	General digital I/O pin
31	P01	General digital I/O pin
32	P00	General digital I/O pin
33	TMS	Digital pin of programming interface
34	TCK	Clock pin of programming interface
35	XIN	External crystal oscillator input pin
36	XOUT	External crystal oscillator output pin
Pin No.	**Pin Name**	**Description**
37	DM	Connected to the DM of USB port
38	DP	Connected to the DP of USB port
39	CC1	Type C CC1 detection pin
40	CC2	Type C CC2 detection pin
41	DVSS	GND
42	DVDD	1.8V
43	VSS	GND
44	VDD5_1	5V input of external power supply
45	VDD5_0	5V input of external power supply
46	DCDC	DCDC power input pin of the chip
47	LX	DCDC power output pin, connected to 6.8 uH inductor
48	VDD5_2	5V input of external power supply

4. Limit Parameters

Parameter	Symbol	Minimum value	Maximum Value	Unit
Voltage range	SW0, SW1	-0.3	30	V
	BST0, BST1	-0.3	36	V
	DRVL0, DRVL1	-0.3	6	V
	DRVH0, DRVH1	-0.3	36	V
	DVDD	-0.3	2	V
	PGND, DVSS, VSS	-0.3	0.3	V
	Other Pin	-0.3	6	V
Junction temperature range	TJ		125	°C
Storage temperature range	Tstg	-40	150	°C
Thermal resistance (from junction temperature to ambient temperature)	θJA	47		°C/W
Human Body Model (HBM)	ESD	-2000	2000	V

5. Recommended Working Conditions

Parameter	Symbol	Minimum value	Typical Value	Maximum Value	Unit
Power supply voltage	DCDC	5.5		25	V
Input voltage range	VDD5	0	5	5.5	V
I/O voltage range	CC1, CC2	0	5	5.5	V
	AMPIN, AMPIP, AMPOT, DP, DM	0	5	5.5	V
	P00–P06, P10–P17	0	5	5.5	V
	ADC0–ADC4,	0	5	5.5	V

Parameter	Symbol	Minimum value	Typical Value	Maximum Value	Unit
	CODE1, CODE2				
	AVDD, nRST, XIN, XOUT, MDAT, MCLK	0	5	5.5	V
Power consumption in standby state	Istandby		10		mA
Working temperature range	TA	-40		85	°C

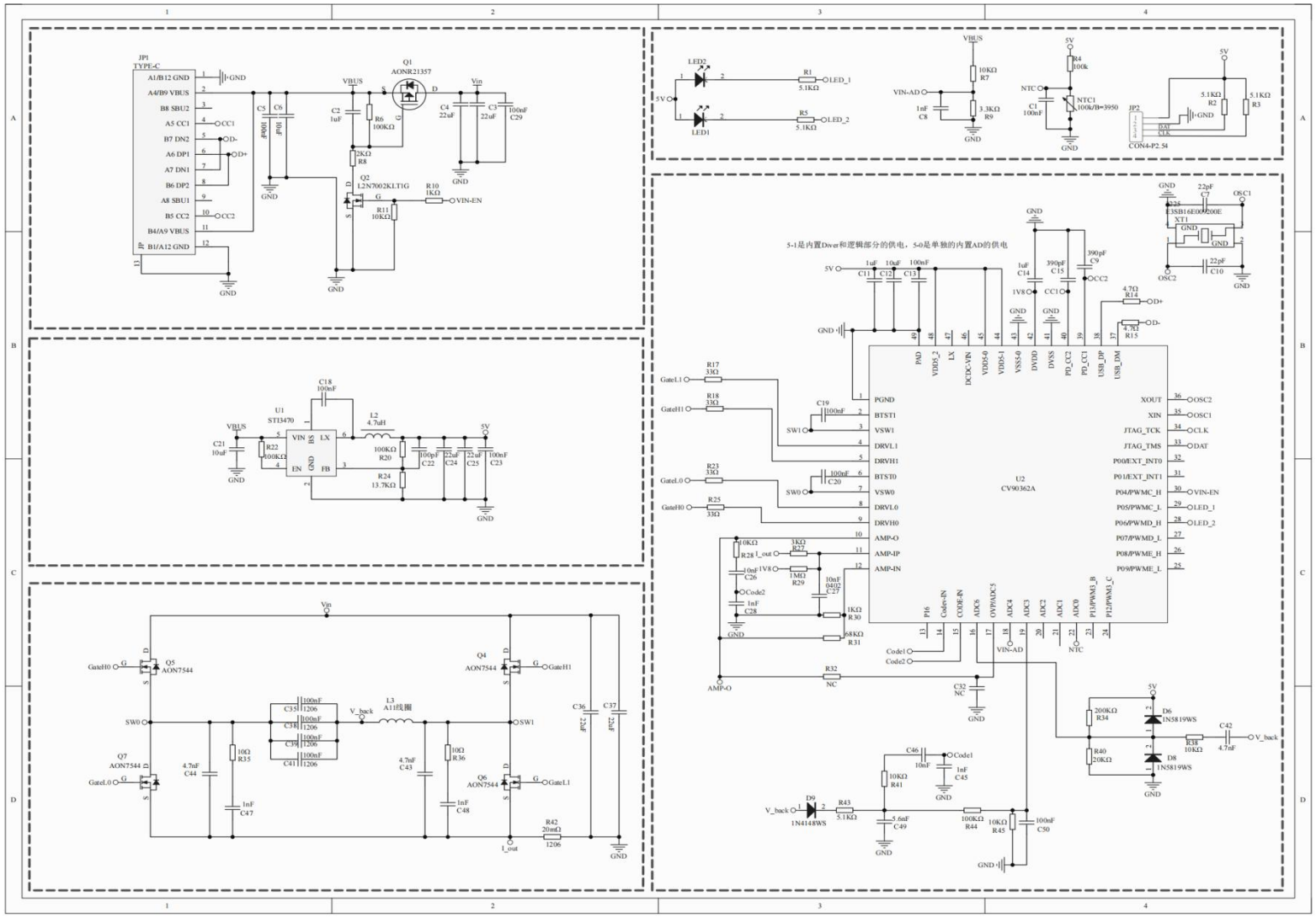
6. Schematic Diagram of Typical Applications

See Page 10.

7. Product Information

The package outline drawing is on the last page of this article.

Model	Package Form	Moisture Resistance Level	Packaging Mode	Minimum Number of Packages
CV90362A	QFN48 (6.00 mm × 6.00 mm × 0.75 mm)	Level 3	Tape	3000 PCS


JP1
TYPE-C
A1/B12 GND
A4/B9 VBUS
B8 SBU2
A5 CC1
B7 DN2
A6 DP1
A7 DN1
B6 DP2
A8 SBU1
B5 CC2
B4/A9 VBUS
B1/A12 GND
Q1
AONR21357
Q2
L2N7002KLT1G
VBUS
Vin
VIN-EN
GND
LED2
LED1
R1 5.1KΩ
R5 5.1KΩ
LED_1
LED_2
VIN-AD
NTC
NTC1 100k/B=3950
JP2
CON4-P2.54
5-1是内置Diver和逻辑部分的供电，5-0是单独的内置AD的供电
U1
ST13470
U2
CV90362A
XOUT
XIN
JTAG_TCK
JTAG_TMS
P00/EXT_INT0
P01/EXT_INT1
P04/PWMC_H
P05/PWMC_L
P06/PWMD_H
P07/PWMD_L
P08/PWME_H
P09/PWME_L
AMP-O
AMP-IP
AMP-IN
GateL1
GateH1
GateL0
GateH0
Q4
AON7544
Q5
AON7544
Q6
AON7544
Q7
AON7544
L3
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V_back
I_out
D6
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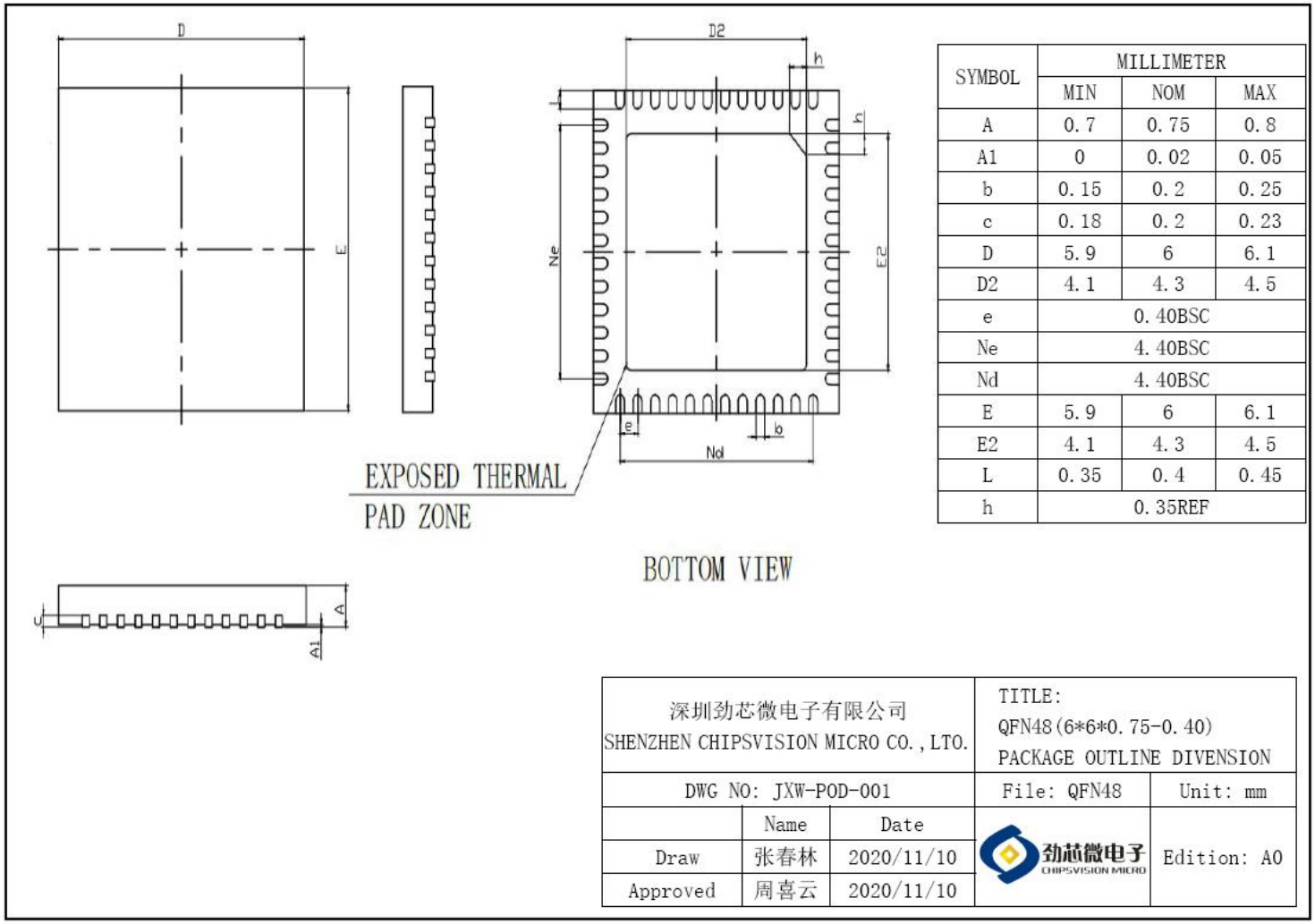
D8
1N5819WS
D9
1N4148WS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
b	0.15	0.2	0.25
c	0.18	0.2	0.23
D	5.9	6	6.1
D2	4.1	4.3	4.5
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.9	6	6.1
E2	4.1	4.3	4.5
L	0.35	0.4	0.45
h	0.35REF		

深圳劲芯微电子有限公司 SHENZHEN CHIPSVISION MICRO CO.,LTO.			TITLE: QFN48(6*6*0.75-0.40) PACKAGE OUTLINE DIVENSION	
DWG NO: JXW-POD-001			File: QFN48	Unit: mm
	Name	Date	劲芯微电子 CHIPSVISION MICRO	Edition: A0
Draw	张春林	2020/11/10		
Approved	周喜云	2020/11/10		