40W Wireless Power Receiver With 5W Transmitter

Description

The CV8085D is a highly-integrated Wireless power single-chip (SoC) with 40W receiver/5W transmitter dual modes, The device can be configured to receiver or transmitter modes, when the devices work in transmitter mode, The rectifier bridge works as a full/half bridge inverts, has a 16bits PWM generator, with dead-zone regulating. Embedded dual channels demodulation for Communication. When device work as receiver mode, The device receivers an AC power from a wireless transmitter, embedded a high efficiency synchronous full bridge rectifier converts to DC power, Embedded modulation and FSK demodulation circuits supports bi-direction communication,

A Microprocessor manages power receiver/transfer and communication, through a I2C port connect with Mobile phones AP, Embedded 16K Bytes MTP memory to support on line debugging and OTA function, low power design to meet the ENERGY star Requirements.

The device includes over-temperature, over-current and over/under voltage protections. The CV8085D is available in 53-WLCSP package.

Wireless power system

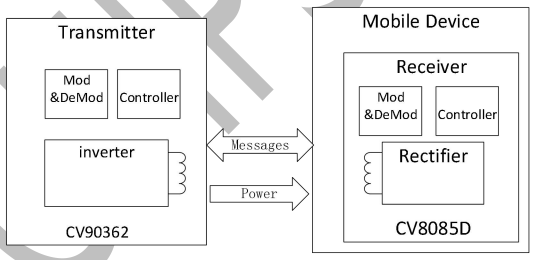


Figure 1

Features

- Single-chip with Rx/TX dual modes wireless power solution
- Compliance with WPC V1.2.4 & V1.3 BPP&EPP
- 16K bytes Multiple-time programmable(MTP) no-volatile memory
- Support private profile/protocol extension
- Support I2C 400KHZ standards interface
- Embedded 12bits high accuracy ADC
- Embedded±1.5% accuracy OSC in full temperature rank
- Low standby and operating power consumption
- 13 GPIOs with 1 channel Capture
- Vrect input voltage up to 36V
- Maximum continuous operating current 3.6A
- Receiver mode
  ---Delivers up to 40W as a receiver
  ---High Efficiency synchronous rectifier with low Rds(on)
  ---Low dropout regulator with low Rds(on)
  ---High accuracy frequency detection for FSK communication
  ---Output Voltage up to 24V, with 20mV regulation/step from 3.6V~24V
  ---Programmable current limit
  ---Programmable Clamping voltage and strength
- Transmitter mode
  ---Up to 5W power delivery
  ---Invert bridge with Half/Full bridge control mode
  ---High accuracy PWM controller to support phase-shift，PWM modulation and dead-zone control
- Package: 6x9 Ball array, 2.7mmx4.0mm, 53-WLCSP with 0.4mm ball pitch

Typical Applications

- Wireless power RTx solution for portable devices
- Mobile phone
- Power bank
- Tablets
- Accessories
- Stationary device power supply

1 System diagram

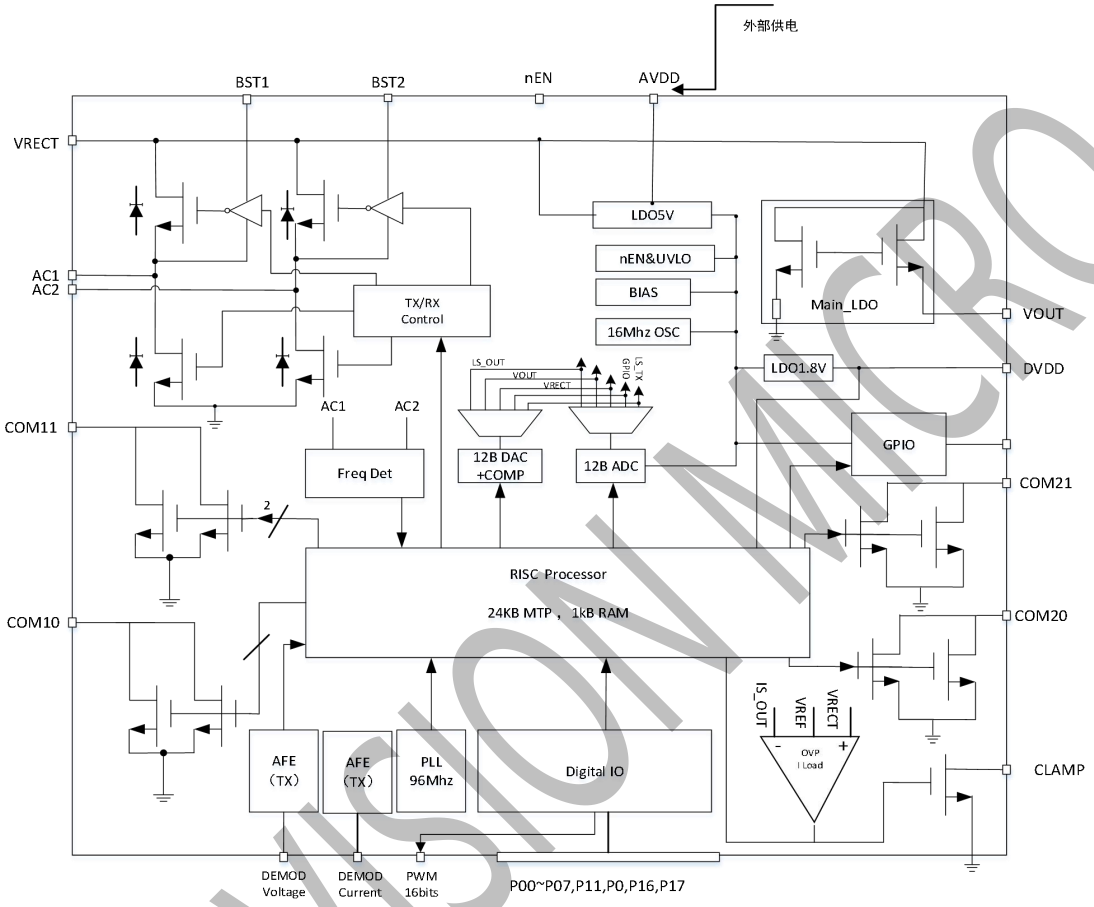


Figure 2

Wireless power system description

The CV8085D is a highly-integrated wireless power transmitter and receiver dual-function IC for mobile or stationary devices, The internal block diagram of CV8085D is shown in figure 2.
The device can transmit up to 5W in WPC Transmitter mode and receiver up to 40W power, It also can support PMA mode (option).

Rx mode

In Rx mode， The device receive the wireless power and stored on Vrect capacitors, until the voltage exceeds the UVLO threshold, the rectification is preformed by the body diodes of Rectifier FETs, Once the internal biasing circuit is working, The CPU can enable high-side FETs, low-side FETs or full bridge ETs to work in switching mode, Depend on system status and power demand. The device uses 12bits ADC to monitor the Vrect and load current, To send instructions to wireless power transmitter

for increasing or decreasing power. The output voltage of low-drop-out regulator (Main LDO) is programmable from 3.6V to 24V with 20mV/step using I2C commands. The OVP, OTP,OCP protection circuit are continuously monitory to ensure system work well。

Tx mode

In Tx mode, The power will input through Vout pin, The processor will control Rectify full bridge to work as inverter bridge, A high resolution PWM can work as 128mHZ to control the inverter bridge work as half/full bridge modes, and dead-zone setting, A high resolution Voltage decoding and A high resolution current decoding to get Rx's instruction through DEMOD filter shown in Figure 3, Based on the receive packet, the CV8085D will adjust the operating frequency to match the transmitted power level to reliable wireless power transfer,
A high resolution PWM controller ensure system in higher efficiency。

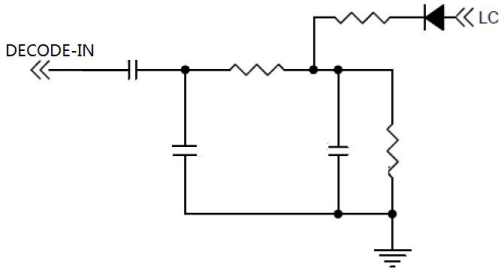


Figure 3

Power Control

The voltage across the Vrect and the current through the rectifier are periodically sampled and digitized by the ADC. The digital equivalent of voltage and current is provided to internal control logic that determines if the operating point needs to be changed based on the load conditions on the Vrect. If the load is heavy enough to cause the voltage at Vrect to be below the target value, the power transmitter is instructed to reduce its frequency, near resonance. If the voltage at Vrect is above its target, the power transmitter is instructed to increase its frequency. To maximize efficiency, the voltage of the Vrect is programmed to decrease as the LDO load current increases.

Power Transfer

When a mobile device containing the CV8085D is placed on the WPC "QI" charging pad, the CV8085D responds to the transmitter's "Ping" signal, completing the "Identification and Configuration". Once the "Identification and Configuration" phase is completed and successfully negotiated and calibrated, the transmitter will initiate the power transfer mode. The CV8085D control circuit measures the Vrect voltage and sends a control error packet to the power transmitter, adjusting the Vrect voltage to achieve optimum efficiency of the LDO. At the same time, the rectifier bridge power data packet is sent to the power transmitter as the basis of the transmitter foreign object detection (FOD) to ensure safe and effective power transmission.

Synchronous Rectifier

The CV8085D's built-in synchronous rectifier bridge can effectively improve the rectification efficiency. When the load is higher than 100mA, the rectifier bridge operates in a synchronous full-bridge rectification manner. When the load is less than 100 mA, the rectifier bridge operates in a semi-synchronous full-bridge rectification mode. During the power-on phase, when the Vrect voltage is lower than the uvlo threshold, the rectifier bridge is fully bridge rectified by the NMOS body diode. The BST capacitor is used to provide a switching drive voltage for the NMOS of the upper bridge.

Advanced Foreign Object Detection（FOD)

When the metal is placed in an alternating magnetic field, the electromagnetic eddy current heats the metal. For example, coins, keys, paper clips, etc. The degree of heating depends on the amplitude and frequency of the coupled magnetic field, as well as the resistible, size and shape of the object. In wireless energy transmission systems, this heat is energy loss, reducing energy transfer efficiency. If proper measures are not taken, metal objects are continuously heated and high temperatures are generated, which may cause other dangerous situations.

In addition, there may be other metals in the final product design of the WPC power transmitter and receiver (these metals are neither part of the power transmitter nor part of the power receiver, but will be from the coupled AC magnetic field during power transmission). Absorbing energy, causing power loss, such as lithium-ion batteries, metal ICs, etc., so FOD detection also needs to compensate for the power loss caused by these metals.

The CV8085D uses advanced FOD technology to detect foreign objects placed on or near the launch pad. The FOD settings can be optimized through an I2C interface or programming to match the power transfer characteristics of each particular WPC system, including power losses for TX and RX coils, batteries, shields, and housing materials from no load to full load. These values are based on a comparison of the received power to the reference power curve so that any foreign matter can be detected when the received power is different than the expected system power.

Over-voltage Protection

If the input voltage increases above setting value (15V、22V、27V), the control loop disables the LDO, sends a control error packet to the power transmitter to attempt to restore the rectifier voltage to a safe operating voltage level, and uses high voltage open drain (Clamp/Sink) to control the OVP FET to the input voltage. Clamping allows Vrect to stabilize. The clamp is released when the Vrect voltage is below the VOVP hysteresis calibration level.

Over temperature、 Over current Protection

Both the over temperature protection threshold and the over current protection threshold of the CV8085D can be programmed. When the output current of the CV8085D exceeds the over current

protection threshold or the detected temperature exceeds the over temperature protection threshold, the CV8085D turns off the LDO output and sends a charge end packet to the power transmitter to terminate the power transfer.

Status Output

GPIO2-4 can be selected to indicate the current working status. For example, charging is completed, charging is abnormal, and the like.

LDO

The CV8085D has three LDOs built in, a high-power LDO, programmable select outputs of 3.6V--24V, VDD5V LDO and VPP18 LDO (VDD5V and VPP18 are both used to power the internal low-voltage operating modules). A filter capacitor is required on each LDO pin.

WPC Mode Communication

Modulation method

According to the WPC specification, in the wireless medium power transmission system, the duplex communication method is adopted: the communication sent by the receiver to the transmitter - the amplitude shift keying (ASK) and the communication sent by the transmitter to the receiver - frequency shift keying (FSK) .

The communication signal sent by the receiver to the transmitter is controlled by the baud rate of 2kpbs to control the external capacitor connected to the internal switch and AC1/AC2 to be grounded or suspended to adjust the load on the receiving induct coil for modulation. This causes the output impedance of the transmitter to change, and this communication signal is ultimately reflected in the resonant amplitude of the transmitting coil. The transmitter acquires communication data by detecting changes in voltage or current on the transmitting coil.

The communication signal sent by the transmitter to the receiver is modulated by changing the frequency of the AC power signal of the transmitter. The receiver detects a frequency change and acquires communication data. A handshake protocol is established with the transmitter through this communication data.

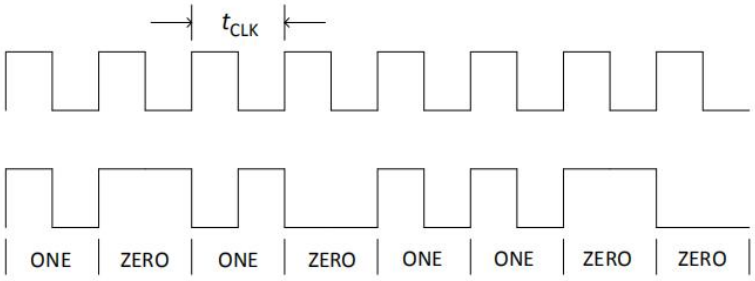
Data Format

According to the WPC specification, the CV8085D communicates with the power transmitter or receiver in the form of data packets. The format of the data packet is as follows:

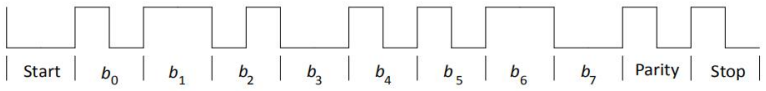
Preamble	Header	Message	Checksum

Encoding

According to the WPC specification, the CV8085D uses a 2 kHz clock frequency to modulate data bits onto the power signal using a two-phase differential encoding. Logic one uses two narrow transforms for encoding, while logic zero uses two wide transforms for encoding, as follows:

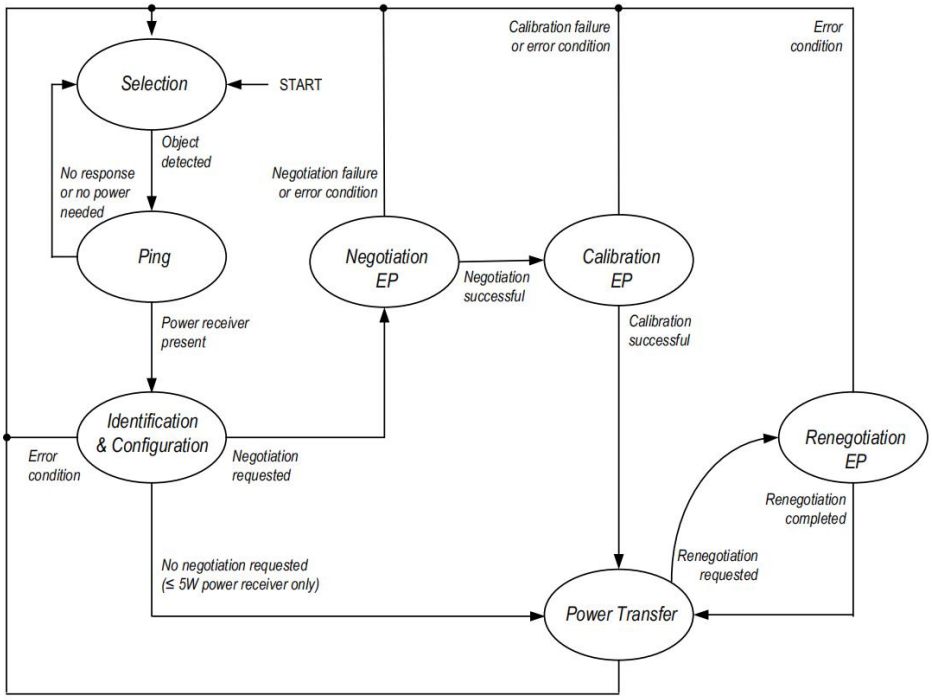


Each byte in the communication packet includes 11 bits in the asynchronous serial format as follows:



System Feedback Control

The CV8085D is fully compatible with WPC (latest specification) and has all the necessary circuitry to communicate with the transmitter or receiver via a WPC communication packet.
The communication process between the transmitter and the receiver is as follows:



ThcCV8085D goes through five phases：
Selection，Ping，Identification & Configuration，Negotiation，Calibration & Power Transfer

Selection

At this stage, the CV8085D receives or transmits wireless power and enters the ping phase. When the Vrect voltage is higher than UVLO, the CV8085D is ready to communicate with the transmitter or enter the power ping mode.

Ping

At this stage, the CV8085D sends a signal strength packet as the first communication packet to instruct the sender to keep the power signal on (or the CV8085D detects the signal strength packet). After transmitting/receiving the signal strength packet, the CV8085D enters the identification and configuration phase. Conversely, if a transport end packet is sent, it will remain in the ping phase.
At this stage, the following two messages are sent/expected:

- Signal strength packet
- End of power packet

Identification & Configuration

At this stage, the following two messages are sent/expected:

- Identification packet
- Configuration packet

NEGOTIATION

The receiver negotiates with the transmitter to adjust the transmitter. In this process, the receiver sends a negotiation request to the transmitter, and the transmitter can agree or reject the negotiation request.

CALIBRATION

At this stage, the receiver provides the received power to the transmitter.

POWER TRANSFER

- At this stage, the CV8085D controls power transfer through the following control packets:
- Control error packet
- Rectified power packet
- End power transfer packet

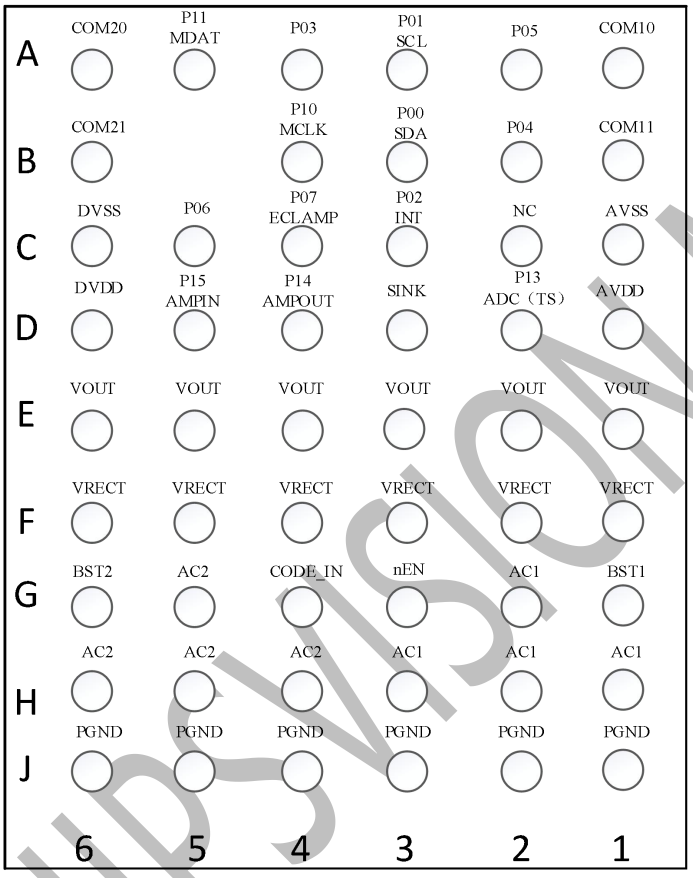
RE-NEGOTIATION

At this stage, the receiver can communicate with the transmitter to adjust if needed. This phase can be terminated early without changing the transmit power.

END OF POWER

When the load on the receiver ends the power request (eg, charging is completed), the CV8085D turns off the LDO output, and continuously transmits the transmission end packet to the transmitter until the transmitter ends the power transmission, or the receiver's Vrect voltage is lower than the UVLO threshold.

2 Pin assignments



Bottom View

3 Pin descriptions

Ball NO	Pin Name	I/0	Description
A1	COM10	O	Communication modulation signal output
A2	P05	I/O	GPIO, Can be set as a 16bits PWM output

Ball NO	Pin Name	I/0	Description
A3	P01 SCL	I/O	I2C clock pin，Open-drain output
A4	P03	I/O	Open Drain GPIO
A5	P11 MDAT	I/O	Program data，Open Drain GPIO
A6	COM20	O	Communication modulation signal output
B1	COM11	O	Communication modulation signal output
B2	P04	I/O	Open Drain GPIO
B3	P00 SDA	I/O	I2C data pin，Open-drain output
B4	P10 MCLK	I	Program CLK，Open Drain GPIO
B5	NC	/	NC
B6	COM21	O	Communication modulation signal output
C1	AVSS	A	Analog GND
C2	NC	/	NC
C3	P02 INT	I/O	Open Drain GPIO
C4	ECLAMP ADC P07	I/O	Open Drain GPIO，Push-Pull output driver for External Power Clamp FET gate control (Connect a resistor from Vrect to the external FET to GND)，This pin can be floating if not used
C5	P06	I/O	Open Drain GPIO, Can be set to capture
C6	DVSS	A	Digital GND
D1	AVDD	A	Internal 5V regulator output voltage，Connect a 1μF capacitor from this pin to ground
D2	ADC(TS) P13	A	Open Drain GPIO，External ADC channel
D3	SINK (CLAMP1)	O	Open drain output for over voltage protection, Which will be trigger, once the Vrect over setting voltage. Connect a resistor from this pin to the Vrect pin, for more detail

			information about over voltage settings, see section 6.1
D4	P14 AMPOUT	A	Open Drain GPIO，Communication signal for current decoding AMP output on TX_mode, This pin can be floating if not used
D5	P15 AMPIN	A	Open Drain GPIO，Current decoding input on TX_mode
D6	DVDD	A	Internal 1.8V regulator output voltage，Connect a 1 μ F capacitor from this pin to ground
E1	VOUT	A	Output voltage to load
E2	VOUT		
E3	VOUT		
E4	VOUT		
E5	VOUT		
E6	VOUT		
F1	VRECT	A	Output voltage of the synchronous rectifier bridge，Connect the capacitors from this pin to GND
F2	VRECT		
F3	VRECT		
F4	VRECT		
F5	VRECT		
F6	VRECT		
G1	BST1	A	Connect a capacitor between BT pin and SW pin to bootstrap a voltage to provide the bias voltage for high side MOSFET gate driver
G2	AC1	A	AC input power，Connect to the resonant capacitor
G3	nEN	I	Chip enable pin
G4	CODE-IN	I	Voltage decoding input on TX_mode
G5	AC2	A	AC input power，Connect to the Rx coil
G6	BST2	A	Connect a capacitor between BT pin and SW pin to bootstrap a voltage to provide the bias voltage for high side MOSFET gate driver
H1	AC1	A	AC input power，Connect to the resonant capacitor

CV8055H2	AC1		
H3	AC1		
H4	AC2	A	AC input power，Connect to the resonant capacitor
H5	AC2		
H6	AC2		
J1	PGND	P	GND
J2	PGND		
J3	PGND		
J4	PGND		
J5	PGND		
J6	PGND		

4 Electrical specification

4.1 Absolute Maximum Ratings

Symbol/Pins	Parameter	Minimum	Maximum	Units
COM21, COM20, COM11, COM10，SINK (CLAMP1), VRECT, AC1, AC2	Maximum voltage	-0.3	36	V
BST1, BST2	Maximum voltage	-0.3	AC1+5,AC2+5	V
DVDD、P05、P04、MDAT、P02、P06、ADC(TS)	Maximum voltage	-0.3	2	V
AVDD、DECODE-IN、nEN、AMPOUT、SCL、MCLK、SDA、P03	Maximum voltage	-0.3	6	V
PGND	Maximum voltage	-0.3	0.3	V
COM21, COM20, COM11, COM10	Maximum RMS current		500	mA
AC1, AC2	Maximum RMS current		3.6	A
VOUT Output Current	Maximum RMS current		3.6	A
HBM	ESD – Human Body Model		2000	V
CDM	ESD – Charged Device Mode		500	V

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

4.2 Thermal Characteristics

Symbol	Parameter	Value	Units
θ_{JA}	Thermal Resistance Junction to Ambient	45	℃/W
θ_{JC}	Thermal Resistance Junction to Case	0.2	℃/W
θ_{JB}	Thermal Resistance Junction to Board	4.36	℃/W
T_J	Operating Junction Temperature	-5 to +150	℃
T_{AMB}	Ambient Operating Temperature	0 to +85	℃
T_{STOR}	Storage Temperature	-55 to +150	℃
T_{BUMP}	Maximum Soldering Temperature (Reflow, Pb-Free)	260	℃

[a] The maximum power dissipation is PD(MAX) = (TJ(MAX) - TA) / θJA where TJ(MAX) is 150°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

[b] This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3″ x 4.5″ in still air conditions.

[c] Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

4.3 Electrical Characteristics Table

Symbol	Description	Conditions	Min	Typ	Max	Units
Input Supplies & UVLO (Tx Mode)						
V_{IN_OUT}	V_{OUT} Input Operating Voltage Range		3.6	5	20	V
VIN_UVLO	Under-Voltage Lockout	VIN Rising	2.6	2.8	3.0	V
		VIN Failing		200		mV
I_{SHD}	Shutdown Current	V_{EN} = V_{IN}		500		uA
Input Current Sense (Tx Mode)						
V_{SEN_OFST}	Amplifier Output Offset voltage	Measured at amplifier output node; V_{ISH} =V_{ISL}		0.6		mV
$ISEN_{ACC\_TYP}$	Measured Current sense accuracy	V_{R_ISNS} =10mV		±2		%
Analog to Digital Converter						
N	Resolution			12		Bit

f_{sample}	Sampling Rate			67.5		kSa/s
Channel	Number of channels			12		
$V_{IN,FS}$	Full scale Input voltage			5		V
Thermal Shutdown						
TSD	Thermal shutdown	Threshold Rising		140		℃
		Threshold Falling		120		℃
Clocks						
F_{LSOSC}	System clock			16		Mhz
General Purpose Inputs/Outputs						
V_{IH}	Input threshold high		1.35			V
V_{IL}	Input threshold low				0.5	V
I_{LKG}	Input Leakage Current	0V and 1.8V	-1		3	uA
V_{OH}	Output logic high	I_{OH} = 4mA, 12mA total	1.44			V
V_{OL}	Output logic low	I_{OL} = 12mA			0.36	V
SCL, SDA (I_2C Interface)						
f_{SCL}	Clock Frequency				400	khz
$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			us
$t_{HD:DAT}$	Data Hold Time		0			ns
t_{LOW}	Clock Low Period		1.3			us
t_{HIGH}	Clock High Period		0.6			us
$t_{SU:STA}$	Set-up Time for Repeated START Condition		0.6			us
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			us
C_B	Capacity Load for Each Bus Line			150		pF
C_I	SCL, SDA Input Capacitance			5		pF
V_{IL}	Input Threshold Low				0.7	V
V_{IH}	Input Threshold High		1.4			V
I_{LKG}	Input Leakage Current	V = 0V and 5V	-1		1	uA
V_{OL}	Output Logic Low	I_{OL} = 12mA			0.36	V

5 Application

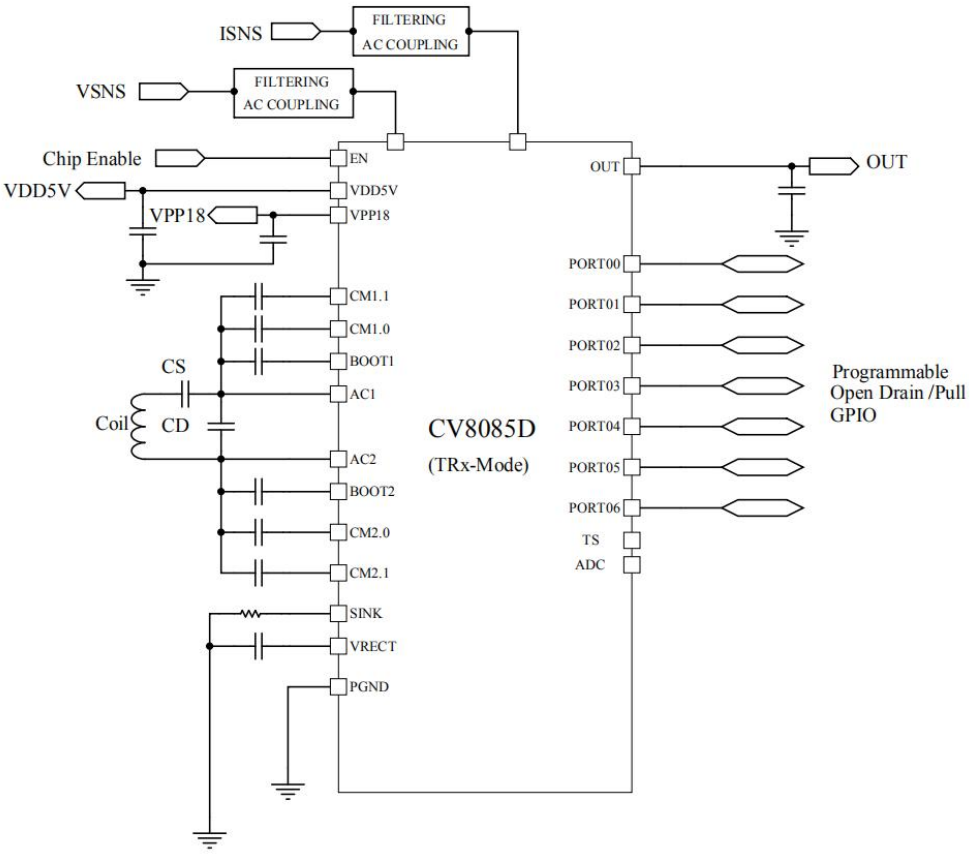


Figure 4

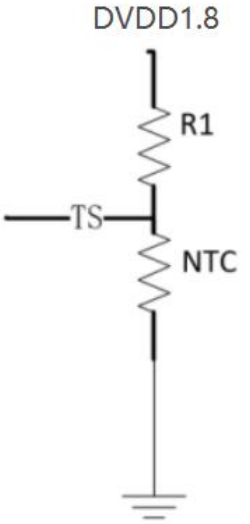
6 Setting and Configuration

6.1 SINK(Clamp1) pin

The CV8085D has embedded a programmable DC clamping to protect the device in the event of high voltage transients, which is a programmable current source, the dissipation capability are 40mA, 80mA, 120mA.

6.2 External Temperature sensing –TS

has a temperature sensor input, TS, which can be used to monitor an external temperature by using a thermistor.



The calculation formula as following: Vts=1.8*NTC/（R1+NTC）

7 Typical Performance Characteristics

The following performance characteristics were taken using a CV90362 wireless power transmitter at Ta=25℃。

7.1 Efficiency 40W（20V@2A)

TX： CV90362，A11 TX Coil，Cs = 400nF，dz=4mm

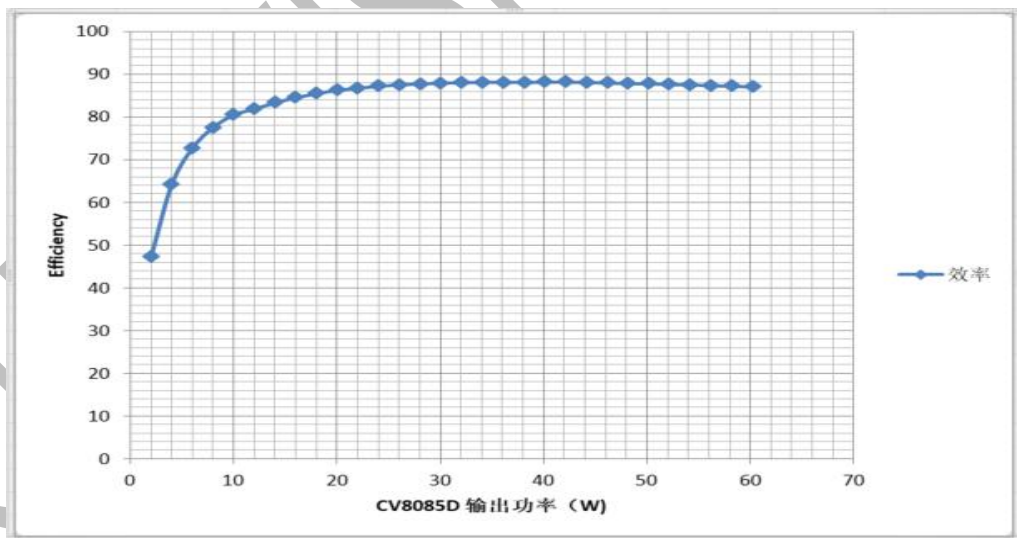


Figure 5. Efficiency vs. Output Power(W)

7.2 Transient Response

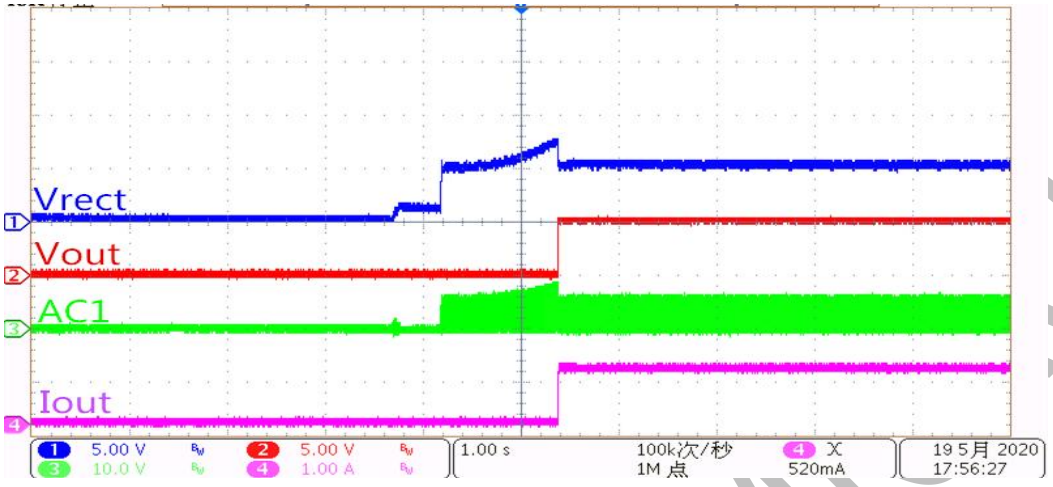


Figure 6. Transient Resp:CV8085D@Vout = 5V， Start up with 1A load

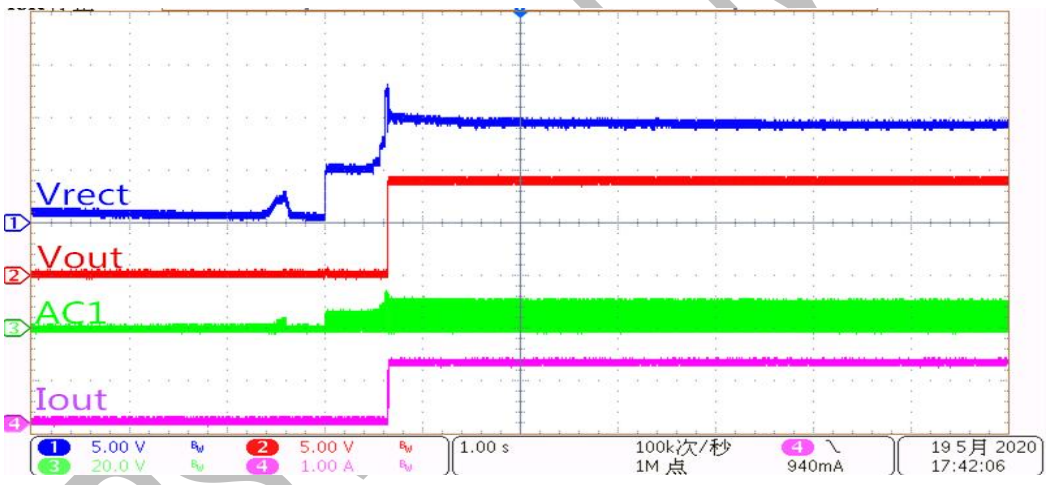


Figure 7. Transient Resp:CV8085D@Vout = 9V，Start up with 1.1A load

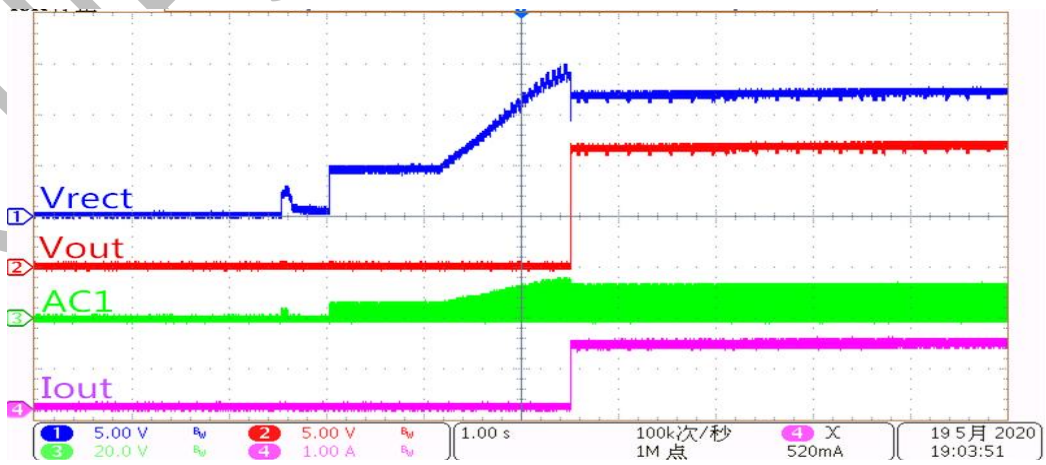


Figure 8. Transient Resp:CV8085D@Vout = 12V，Start up with 1.25A load

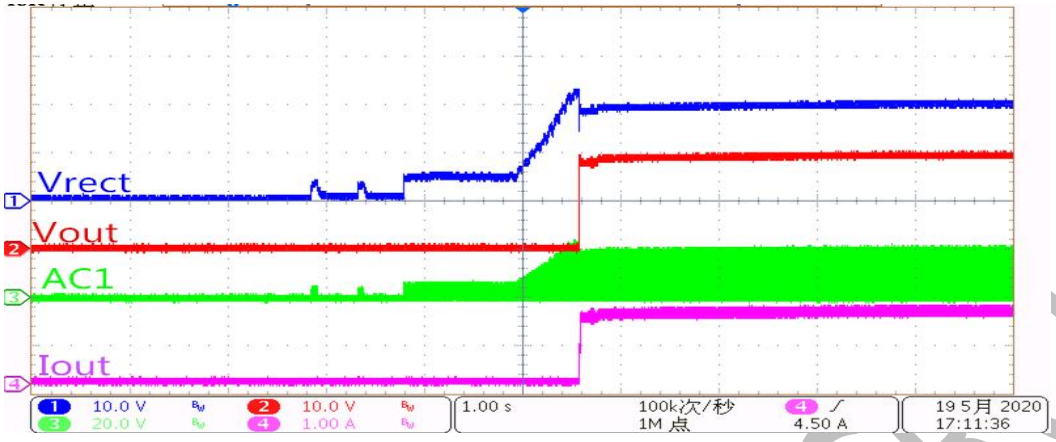


Figure 9. Transient Resp:CV8085D@Vout = 20V，Start up with 1.5A load

7.3 OVP protection

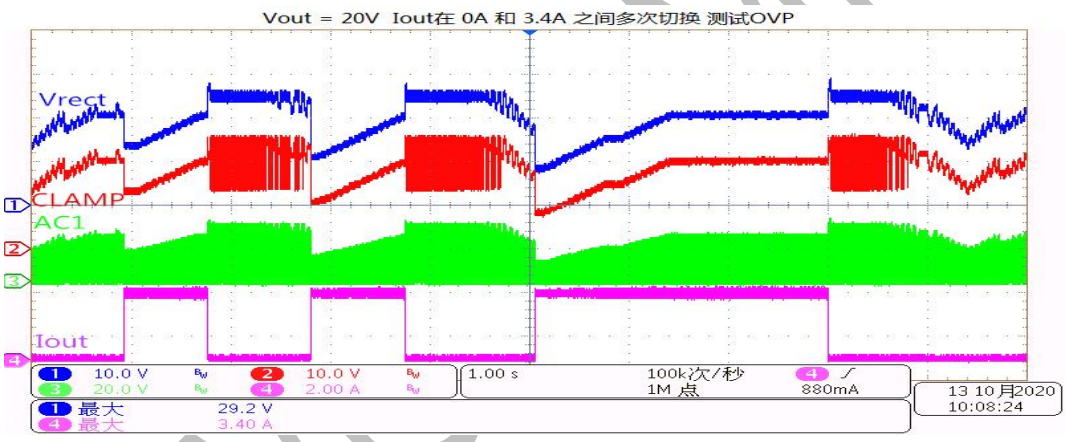


Figure 10. CV8085D@Vout = 20V，3.4A to 0A load for testing OVP

7.4 OCP protection

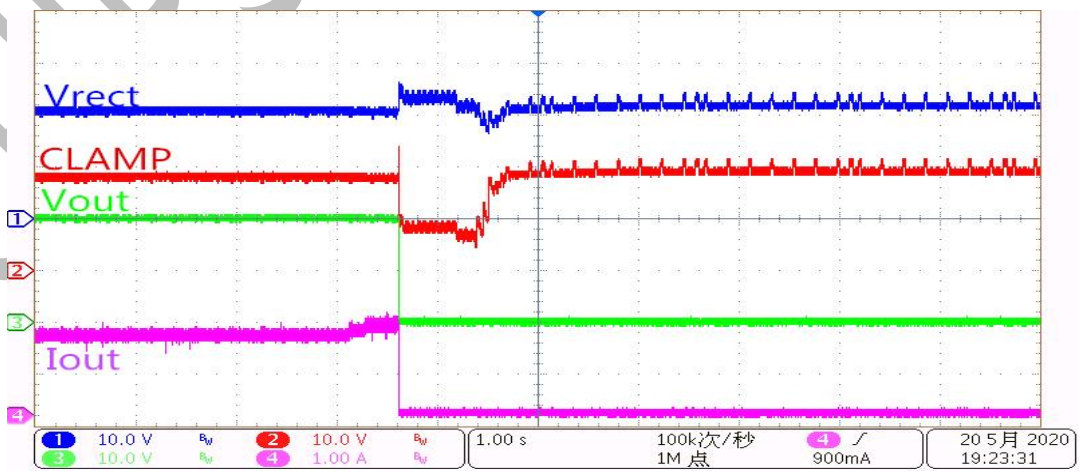


Figure 11. CV8085D@Vout = 20V，OCP @load = 1.7A

8 Application circuit

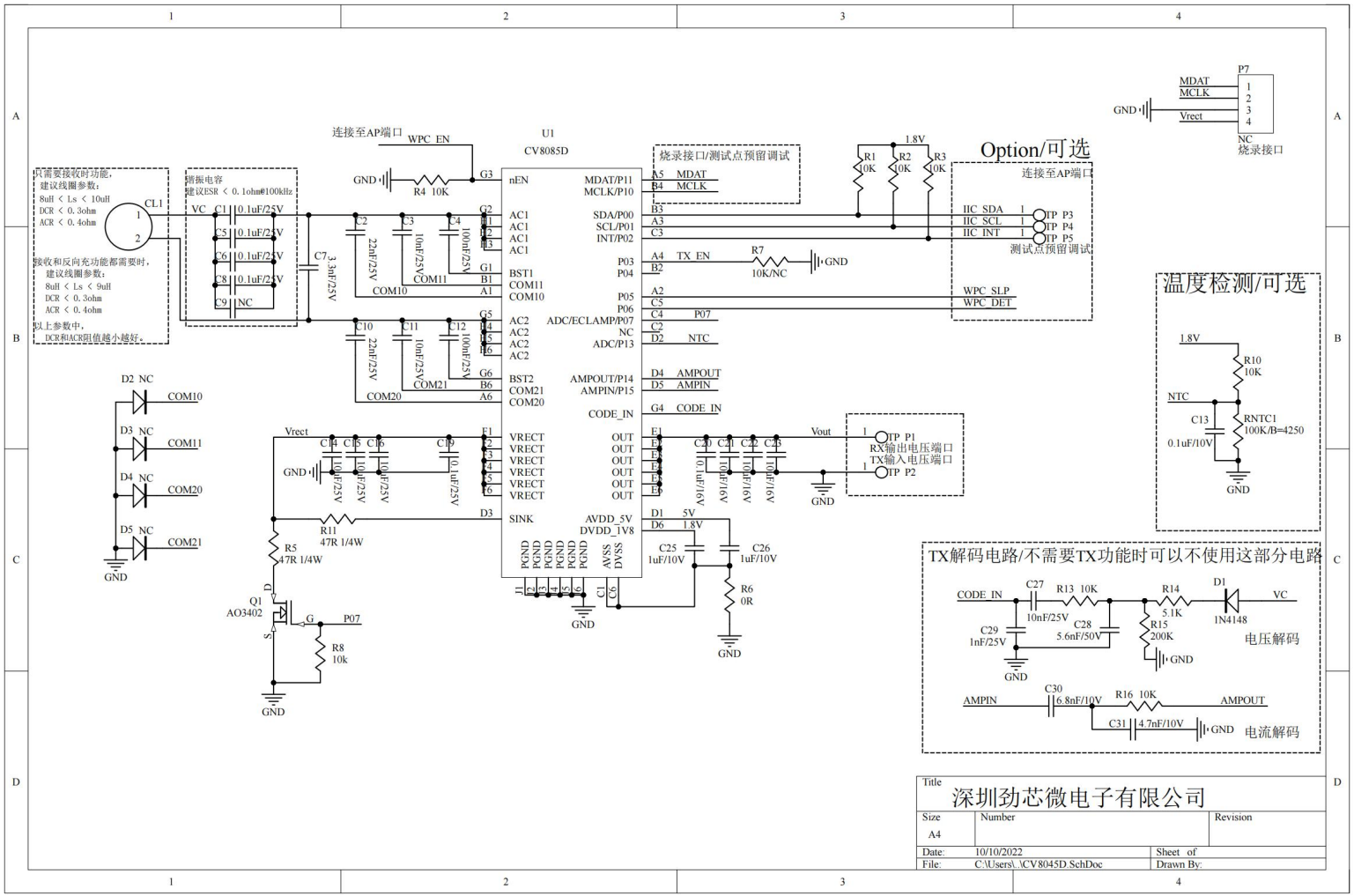
The circuit reference design is on page 19 of this document.

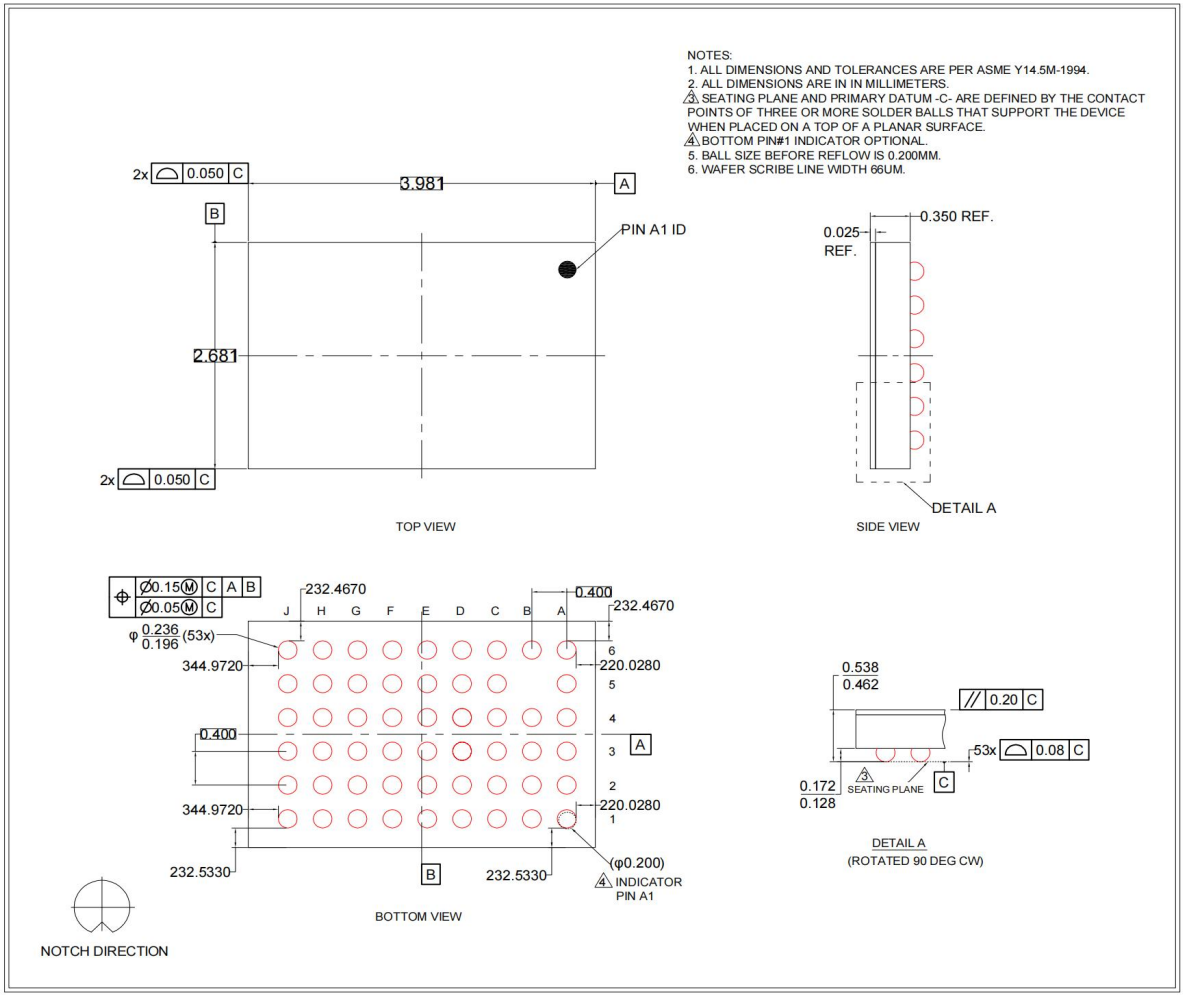
9 Package info

The package outline drawings are appended at the end of this document.

10 Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Shipping Packaging	Ambient Temperature
CV8085D	CV8085D Wireless Power Receiver for 40W & 5WTX Applications, 2.7 X 4.0 mm WLCSP-53	MSL1	Tape and reel	0°C to +85°C


U1
CV8085D
连接至AP端口
WPC_EN
烧录接口/测试点预留调试
Option/可选
连接至AP端口
测试点预留调试
温度检测/可选
TX解码电路/不需要TX功能时可以不使用这部分电路
电压解码
电流解码
深圳劲芯微电子有限公司
Title
Size
A4
Number
Revision
Date: 10/10/2022
Sheet of
File: C:\Users\..\CV8045D.SchDoc
Drawn By:


NOTES:
1. ALL DIMENSIONS AND TOLERANCES ARE PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN IN MILLIMETERS.
3. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE CONTACT POINTS OF THREE OR MORE SOLDER BALLS THAT SUPPORT THE DEVICE WHEN PLACED ON A TOP OF A PLANAR SURFACE.
4. BOTTOM PIN#1 INDICATOR OPTIONAL.
5. BALL SIZE BEFORE REFLOW IS 0.200MM.
6. WAFER SCRIBE LINE WIDTH 66UM.
2x 0.050 C
3.981
A
B
PIN A1 ID
2.681
2x 0.050 C
TOP VIEW
0.350 REF.
0.025 REF.
DETAIL A
SIDE VIEW
Ø0.15 M C A B
Ø0.05 M C
232.4670
0.400
232.4670
J H G F E D C B A
φ 0.236 0.196 (53x)
344.9720
220.0280
6
5
4
0.400
3
A
2
344.9720
220.0280
1
232.5330
B
232.5330
(φ0.200)
4 INDICATOR PIN A1
BOTTOM VIEW
NOTCH DIRECTION
0.538
0.462
0.20 C
53x 0.08 C
0.172
0.128
3 SEATING PLANE
C
DETAIL A
(ROTATED 90 DEG CW)