15W Wireless Power Receiver Control SOC

Description

The CV8015 is a highly-integrated Wireless power single-chip (SoC) with 15W receiver,Compliance with WPC V1.2.4&V1.3 BPP&EPP,Internal integration of efficient full synchronous rectifier, low voltage drop regulator (LDO), can achieve a single chip non-contact wireless charging receiving scheme.

The CV8015 features Multiple-time programmable (MTP) nonvolatile memory to easily update control firmware and device functions.The device includes over-temperature and voltage protection.. The chip reserves two general serial ports, both of which can realize standard dual-line communication; And contains 12 GPIO, provides a flexible solution for system development.

Typical Applications

- Wireless power Rx solution for portable devices
- Mobile phone
- Power bank
- Tablets
- Accessories
- Stationary device power supply

Features

- Highly integrated 15W wireless charging receiver chip
- Compliance with WPC V1.2.4&V1.3 BPP&EPP
- 16K bytes Multiple-time programmable(MTP) no-volatile memory
- Support private profile/protocol extension
- Support I2C 400KHZ standards interface,12 GPIOs with 1 channel Capture
- Embedded 2 12bits high accuracy ADC
- Embedded±1.5% accuracy OSC in full temperature rank
- Low standby and operating power consumption
- Vrect input voltage up to 20V,with 20mV regulation/step from 3.6V~20V
- Reliable over voltage clamping
- Maximum continuous operating current 1.5A and Programmable current limit
- High Efficiency synchronous rectifier ,Low dropout regulator with low Rds(on)
- Support High accuracy frequency detection for FSK communication
- Package: 6mm * 6mm *0.75mm,QFN48.

Wireless power system

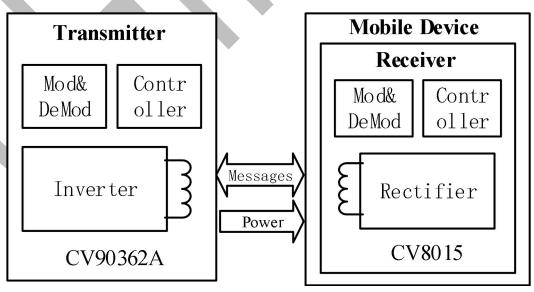


Figure 1

1 System diagram

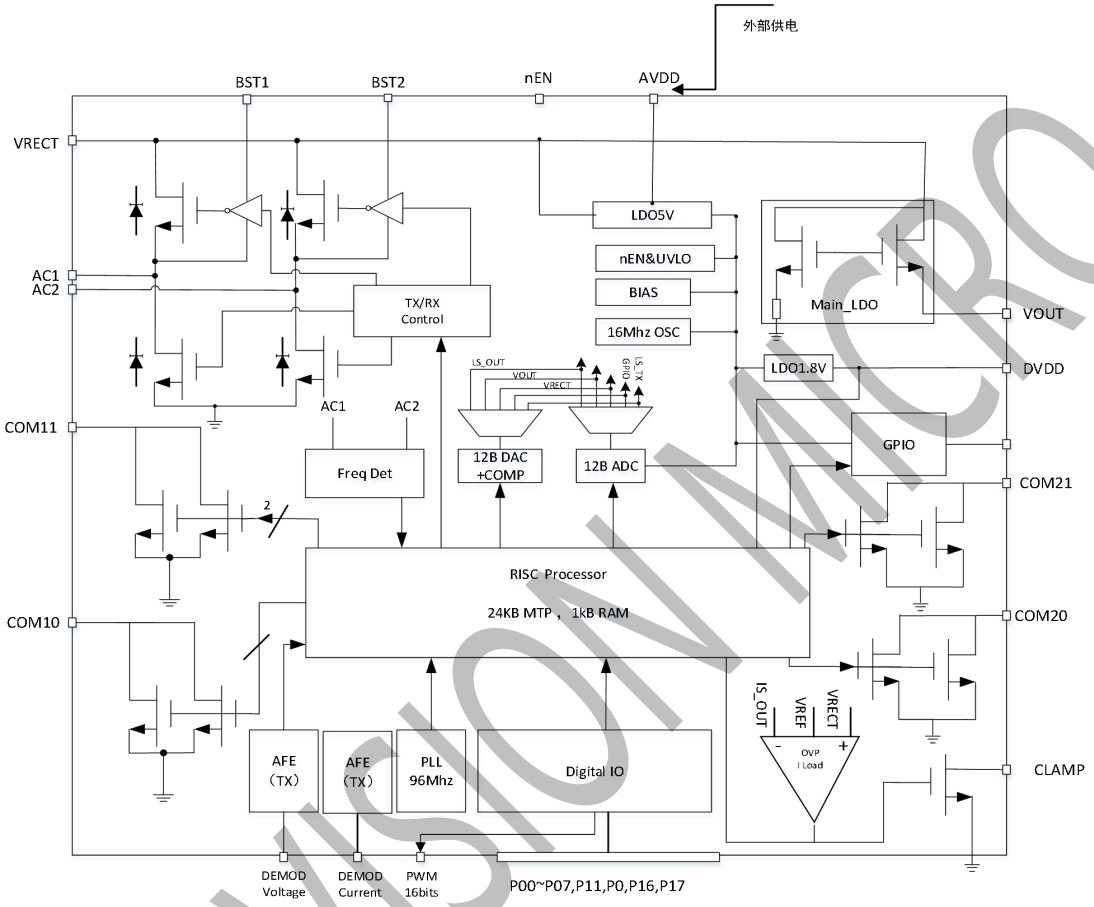


Figure 2

Wireless power system description

The CV8015 is a highly integrated wireless power receiver IC,s, The internal block diagram of CV8015 is shown in figure 2.The device can transmit up to 5W in WPC Transmitter mode and receiver up to 15W power, It also can support PMA mode (option).

Rx mode

In Rx mode， The device receive the wireless power and stored on Vrect capacitors, until the voltage exceeds the UVLO threshold, the rectification is preformed by the body diodes of Rectifier FETs, Once the internal biasing circuit is working, The CPU can enable high-side FETs, low-side FETs or full bridge ETs to work in switching mode, Depend on system status and power demand. The device uses 12bits ADC to monitor the Vrect and load current, To send instructions to wireless power transmitter for increasing or decreasing power. The output voltage of low-drop-out regulator (Main LDO) is programmable from 3.6V to 20V with 20mV/step using I2C commands. The OVP, OTP,OCP

protection circuit are continuously monitory to ensure system work well。

Power Control

The voltage across the Vrect and the current through the rectifier are periodically sampled and digitized by the ADC. The digital equivalent of voltage and current is provided to internal control logic that determines if the operating point needs to be changed based on the load conditions on the Vrect. If the load is heavy enough to cause the voltage at Vrect to be below the target value, the power transmitter is instructed to reduce its frequency, near resonance. If the voltage at Vrect is above its target, the power transmitter is instructed to increase its frequency. To maximize efficiency, the voltage of the Vrect is programmed to decrease as the LDO load current increases.

Power Transfer

When a mobile device containing the CV8015 is placed on the WPC "QI" charging pad, the CV8015 responds to the transmitter's "Ping" signal, completing the "Identification and Configuration". Once the "Identification and Configuration" phase is completed and successfully negotiated and calibrated, the transmitter will initiate the power transfer mode. The CV8015 control circuit measures the Vrect voltage and sends a control error packet to the power transmitter, adjusting the Vrect voltage to achieve optimum efficiency of the LDO. At the same time, the rectifier bridge power data packet is sent to the power transmitter as the basis of the transmitter foreign object detection (FOD) to ensure safe and effective power transmission.

Synchronous Rectifier

The CV8015's built-in synchronous rectifier bridge can effectively improve the rectification efficiency. When the load is higher than 100mA, the rectifier bridge operates in a synchronous full-bridge rectification manner. When the load is less than 100 mA, the rectifier bridge operates in a semi-synchronous full-bridge rectification mode. During the power-on phase, when the Vrect voltage is lower than the uvlo threshold, the rectifier bridge is fully bridge rectified by the NMOS body diode. The BST capacitor is used to provide a switching drive voltage for the NMOS of the upper bridge.

Advanced Foreign Object Detection (FOD)

When the metal is placed in an alternating magnetic field, the electromagnetic eddy current heats the metal. For example, coins, keys, paper clips, etc. The degree of heating depends on the amplitude and frequency of the coupled magnetic field, as well as the resistible, size and shape of the object. In wireless energy transmission systems, this heat is energy loss, reducing energy transfer efficiency. If proper measures are not taken, metal objects are continuously heated and high temperatures are generated, which may cause other dangerous situations.

In addition, there may be other metals in the final product design of the WPC power transmitter and receiver (these metals are neither part of the power transmitter nor part of the power receiver, but will be from the coupled AC magnetic field during power transmission). Absorbing energy, causing

power loss, such as lithium-ion batteries, metal ICs, etc., so FOD detection also needs to compensate for the power loss caused by these metals.

The CV8015 uses advanced FOD technology to detect foreign objects placed on or near the launch pad. The FOD settings can be optimized through an I2C interface or programming to match the power transfer characteristics of each particular WPC system, including power losses for TX and RX coils, batteries, shields, and housing materials from no load to full load. These values are based on a comparison of the received power to the reference power curve so that any foreign matter can be detected when the received power is different than the expected system power.

Over-voltage Protection

If the input voltage increases above setting value (15V、22V、27V）, the control loop disables the LDO, sends a control error packet to the power transmitter to attempt to restore the rectifier voltage to a safe operating voltage level, and uses high voltage open drain (Clamp/Sink) to control the OVP FET to the input voltage. Clamping allows Vrect to stabilize. The clamp is released when the Vrect voltage is below the VOVP hysteresis calibration level.

Over temperature、 Over current Protection

Both the over temperature protection threshold and the over current protection threshold of the CV8015 can be programmed. When the output current of the CV8015 exceeds the over current protection threshold or the detected temperature exceeds the over temperature protection threshold, the CV8015 turns off the LDO output and sends a charge end packet to the power transmitter to terminate the power transfer.

Status Output

GPIO2-4 can be selected to indicate the current working status. For example, charging is completed, charging is abnormal, and the like.

LDO

The CV8015 has three LDOs built in, a high-power LDO, programmable select outputs of 3.6V--20V, VDD5V LDO and VPP18 LDO (VDD5V and VPP18 are both used to power the internal low-voltage operating modules). A filter capacitor is required on each LDO pin.

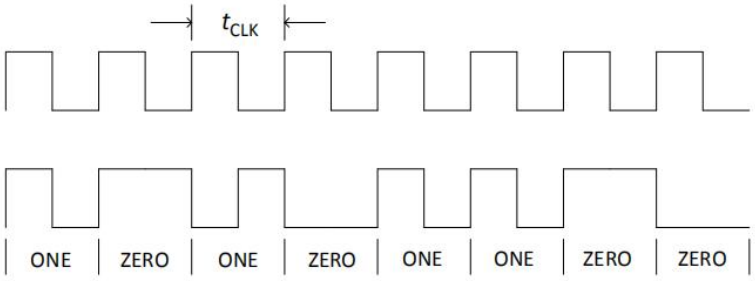
Data Format

According to the WPC specification, the CV8015 communicates with the power transmitter or receiver in the form of data packets. The format of the data packet is as follows:

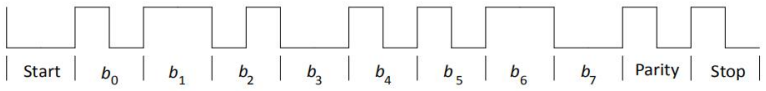
Preamble	Header	Message	Checksum

Encoding

According to the WPC specification, the CV8015 uses a 2 kHz clock frequency to modulate data bits onto the power signal using a two-phase differential encoding. Logic one uses two narrow transforms for encoding, while logic zero uses two wide transforms for encoding, as follows:

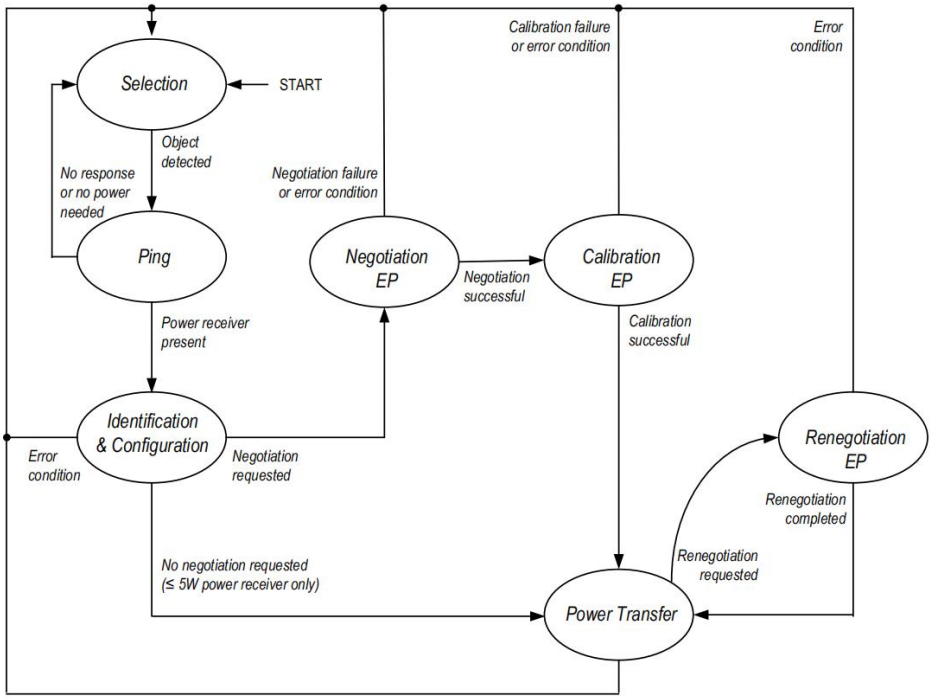


Each byte in the communication packet includes 11 bits in the asynchronous serial format as follows:



System Feedback Control

The CV8015 is fully compatible with WPC (latest specification) and has all the necessary circuitry to communicate with the transmitter or receiver via a WPC communication packet.
The communication process between the transmitter and the receiver is as follows:



ThcCV8015 goes through five phases：

Selection，Ping，Identification & Configuration，Negotiation，Calibration & Power Transfer

Selection

At this stage, the CV8015 receives or transmits wireless power and enters the ping phase. When the Vrect voltage is higher than UVLO, the CV8015 is ready to communicate with the transmitter or enter the power ping mode.

Ping

At this stage, the CV8015 sends a signal strength packet as the first communication packet to instruct the sender to keep the power signal on (or the CV8015 detects the signal strength packet). After transmitting/receiving the signal strength packet, the CV8015 enters the identification and configuration phase. Conversely, if a transport end packet is sent, it will remain in the ping phase.
At this stage, the following two messages are sent/expected:

- Signal strength packet
- End of power packet

Identification & Configuration

At this stage, the following two messages are sent/expected:

- Identification packet
- Configuration packet

NEGOTIATION

The receiver negotiates with the transmitter to adjust the transmitter. In this process, the receiver sends a negotiation request to the transmitter, and the transmitter can agree or reject the negotiation request.

CALIBRATION

At this stage, the receiver provides the received power to the transmitter.

POWER TRANSFER

- At this stage, the CV8015 controls power transfer through the following control packets:
- Control error packet
- Rectified power packet
- End power transfer packet

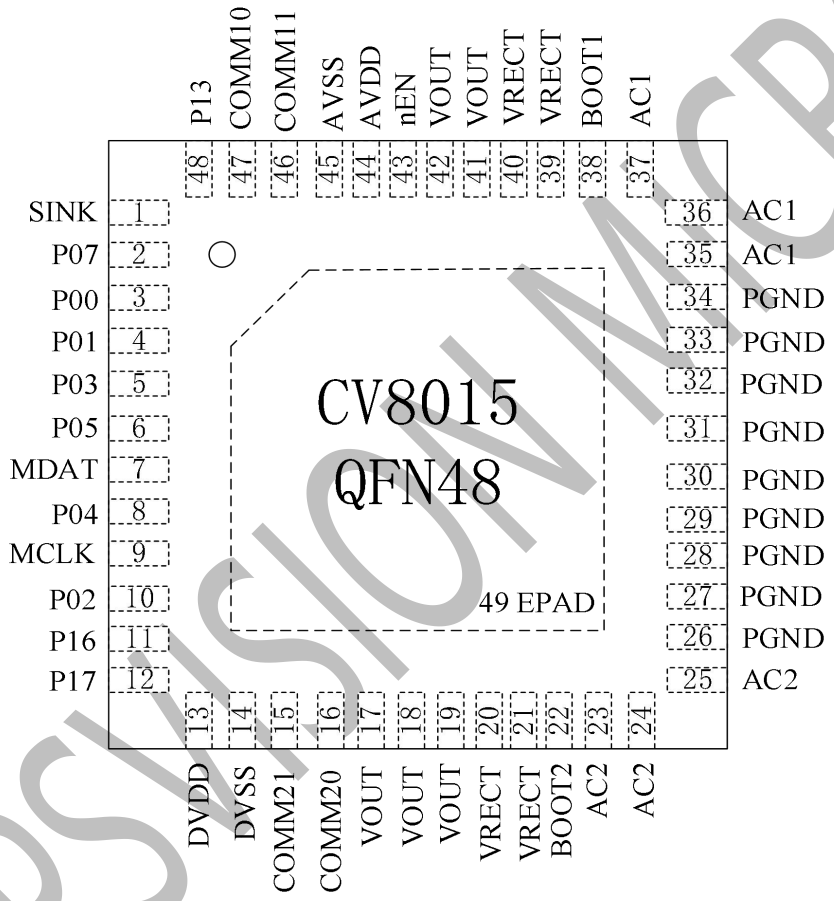
RE-NEGOTIATION

At this stage, the receiver can communicate with the transmitter to adjust if needed. This phase can be terminated early without changing the transmit power.

END OF POWER

When the load on the receiver ends the power request (eg, charging is completed), the CV8015 turns off the LDO output, and continuously transmits the transmission end packet to the transmitter until the transmitter ends the power transmission, or the receiver's Vrect voltage is lower than the UVLO threshold.

2 Pin assignments



3 Pin descriptions

Pin NO.	Pin Name	Description
1	SINK CLAMP1	Open drain output for over voltage protection, Which will be trigger, once the Vrect over setting voltage. Connect a resistor from this pin to the Vrect pin, for more detail information about over voltage settings, see section 6.1
2	P07 ECLAMP ADC	Push-Pull output driver for External Power Clamp FET gate control (Connect a resistor from Vrect to the external FET to GND). This pin can be floating if not used.

3	P00 SDA	I2C data pin. Open-drain output. Connect a 5.1kΩ resistor to VDD18 pin.
4	P01 SCL	I2C clock pin. Open-drain output. Connect a 5.1kΩ resistor to VDD18 pin.
5	P03	Open Drain GPIO
6	P05	Open Drain GPIO
7	MDAT P11	Program data Open Drain GPIO
8	P04	Open Drain GPIO
9	MCLK P10	Program CLK, connect a 10K Ω resistor to VDD18 pin. Open Drain GPIO
10	P02 INT	Open Drain GPIO
11	P16	Open Drain GPIO
12	P17	Open Drain GPIO
13	DVDD	Internal 1.8V regulator output voltage
14	DVSS	Digital GND
15	COMM2[1]	Communication modulation signal output
16	COMM2[0]	Communication modulation signal output
17	VOUT	Output voltage to load
18	VOUT	Output voltage to load
19	VOUT	Output voltage to load
20	VRECT	Output voltage of the synchronous rectifier bridge. Connect three 10μF capacitors from this pinto GND
21	VRECT	Output voltage of the synchronous rectifier bridge. Connect three 10μF capacitors from this pinto GND
22	BOOT2	Boost capacitor for driving the high-side switch of the internal rectifier. Connect a 15nF capacitor from the AC1 pin to B00T1
23	AC2	AC input power. Connect to the resonant capacitor
24	AC2	AC input power. Connect to the resonant capacitor

25	AC2	AC input power. Connect to the resonant capacitor
26	PGND	GND
27	PGND	GND
28	PGND	GND
29	PGND	GND
30	PGND	GND
31	PGND	GND
32	PGND	GND
33	PGND	GND
34	PGND	GND
35	AC1	AC input power. Connect to the resonant capacitor
36	AC1	AC input power. Connect to the resonant capacitor
37	AC1	AC input power. Connect to the resonant capacitor
38	BOOT1	Boost capacitor for driving the high-side switch of the internal rectifier, Connect a 15nF capacitor from the AC2 pin to B00T2
39	VRECT	Output voltage of the synchronous rectifier bridge. Connect three 10μF capacitors from this pinto GND
40	VRECT	Output voltage of the synchronous rectifier bridge. Connect three 10μF capacitors from this pinto GND
41	VOUT	Output voltage to load
42	VOUT	Output voltage to load
43	nEN	Chip enable pin
44	AVDD	Internal 5V regulator output voltage. Connect a 1μF capacitor from this pin to ground.
45	AVSS	Analog GND
46	COMM1[1]	Communication modulation signal output（Reserved）
47	COMM1[0]	Communication modulation signal output
48	P13 ADC TS	External ADC channel
49	PGND	GND

4 Electrical specification

4.1 Absolute Maximum Ratings

Symbol/Pins	Parameter	Minimum	Maximum	Units
COM21, COM20, COM11, COM10, SINK (CLAMP1), VRECT, AC1, AC2	Maximum voltage	-0.3	36	V
BOOT1, BOOT2	Maximum voltage	-0.3	AC1+5,AC2+5	V
DVDD、P04、MDAT、P02/INT、P06、ADC(TS)	Maximum voltage	-0.3	2	V
PGND	Maximum voltage	-0.3	0.3	V
Other Pin	Maximum voltage	-0.3	6	V
COMM2[1], COMM2[0], COMM1[1], COMM1[0]	Maximum RMS current		500	mA
AC1, AC2	Maximum RMS current		3.6	A
VOUT Output Current	Maximum RMS current		3.6	A
HBM	ESD – Human Body Model		2000	V
CDM	ESD – Charged Device Mode		500	V

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

4.2 Thermal Characteristics

Symbol	Parameter	Value	Units
θ_{JA}	Thermal Resistance Junction to Ambient	45	℃/W
θ_{JC}	Thermal Resistance Junction to Case	0.2	℃/W
θ_{JB}	Thermal Resistance Junction to Board	4.36	℃/W
T_J	Operating Junction Temperature	-5 to +150	℃
T_{AMB}	Ambient Operating Temperature	0 to +85	℃
T_{STOR}	Storage Temperature	-55 to +150	℃
T_{BUMP}	Maximum Soldering Temperature (Reflow, Pb-Free)	260	℃

[a] The maximum power dissipation is PD(MAX) = (TJ(MAX) - TA) / θJA where TJ(MAX) is 150°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

[b] This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3″ x

4.5″ in still air conditions.

[c] Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

4.3 Electrical Characteristics Table

Symbol	Description	Conditions	Min	Typ	Max	Units
Input Supplies & UVLO (Tx Mode)						
V_{IN_OUT}	V_{OUT} Input Operating Voltage Range		3.6	5	20	V
VIN_UVLO	Under-Voltage Lockout	VIN Rising	2.6	2.8	3.0	V
		VIN Failing		200		mV
I_{SHD}	Shutdown Current	V_{EN} = V_{IN}		500		uA
Input Current Sense (Tx Mode)						
V_{SEN_OFST}	Amplifier Output Offset voltage	Measured at amplifier output node; V_{ISH} =V_{ISL}		0.6		mV
$ISEN_{ACC\_TYP}$	Measured Current sense accuracy	V_{R_ISNS} =10mV		±2		%
Analog to Digital Converter						
N	Resolution			12		Bit
f_{sample}	Sampling Rate			67.5		kSa/s
Channel	Number of channels			12		
$V_{IN,FS}$	Full scale Input voltage			5		V
Thermal Shutdown						
TSD	Thermal shutdown	Threshold Rising		140		℃
		Threshold Falling		120		℃
Clocks						
F_{LSOSC}	System clock			16		Mhz
General Purpose Inputs/Outputs						
V_{IH}	Input threshold high		1.35			V
V_{IL}	Input threshold low				0.5	V
I_{LKG}	Input Leakage Current	0V and 1.8V	-1		3	uA
V_{OH}	Output logic high	I_{OH} = 4mA, 12mA total	1.44			V
V_{OL}	Output logic low	I_{OL} = 12mA			0.36	V
SCL, SDA (I_2C Interface)						
f_{SCL}	Clock Frequency				400	khz

$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			us
$t_{HD:DAT}$	Data Hold Time		0			ns
t_{LOW}	Clock Low Period		1.3			us
t_{HIGH}	Clock High Period		0.6			us
$t_{SU:STA}$	Set-up Time for Repeated START Condition		0.6			us
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			us
C_B	Capacity Load for Each Bus Line			150		pF
C_I	SCL, SDA Input Capacitance			5		pF
V_{IL}	Input Threshold Low				0.7	V
V_{IH}	Input Threshold High		1.4			V
I_{LKG}	Input Leakage Current	V = 0V and 5V	-1		1	uA
V_{OL}	Output Logic Low	I_{OL} = 12mA			0.36	V

5 Application

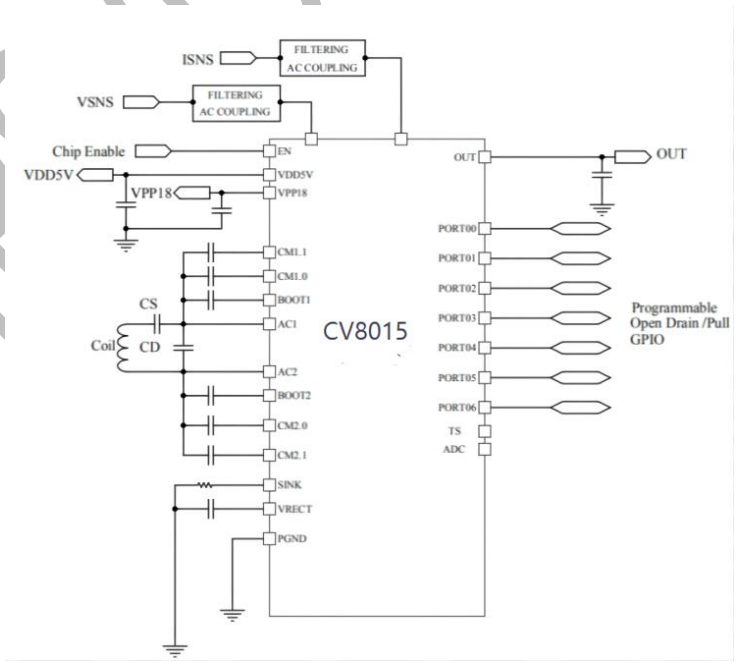


Figure 4

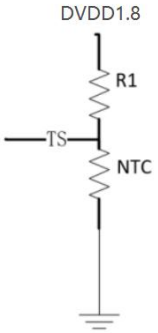
6 Setting and Configuration

6.1 SINK(Clamp1) pin

The CV8015 has embedded a programmable DC clamping to protect the device in the event of high voltage transients, which is a programmable current source, the dissipation capability are 40mA, 80mA, 120mA.

6.2 External Temperature sensing –TS

has a temperature sensor input, TS, which can be used to monitor an external temperature by using a thermistor.



The calculation formula as following: Vts=1.8*NTC/（R1+NTC）

7 Typical Performance Characteristics

The following performance characteristics were taken using a CV90362 wireless power transmitter at Ta=25℃。

7.1 Efficiency 15W（12V@1.25A)

TX： CV90362，A11 TX Coil，Cs = 400nF，dz=4mm

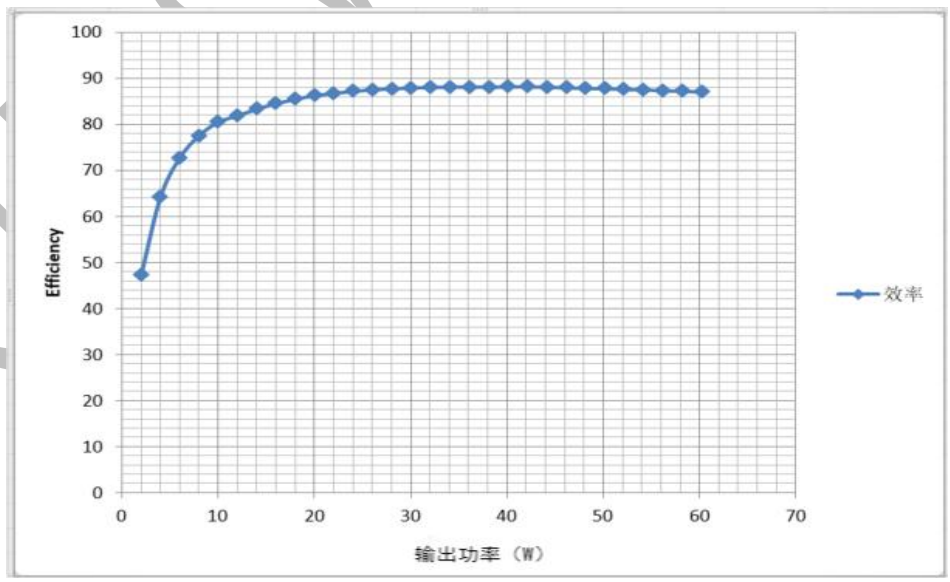


Figure 5. Efficiency vs. Output Power(W)

7.2 Transient Response

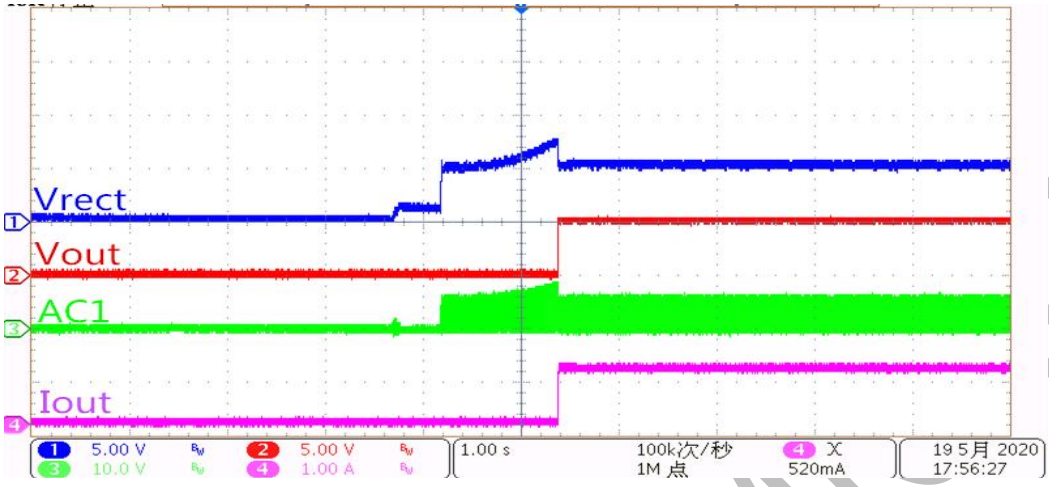


Figure 6. Transient Resp:CV8015@Vout = 5V， Start up with 1A load

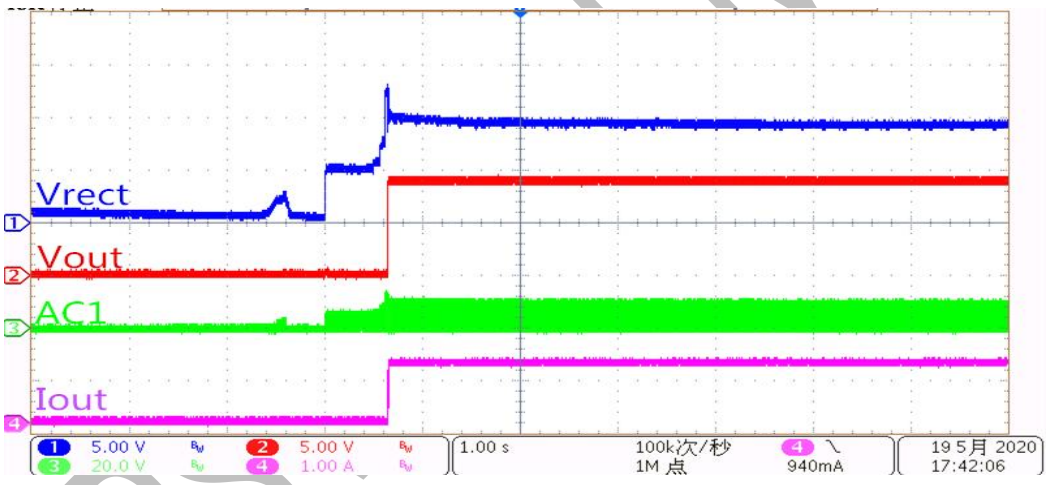


Figure 7. Transient Resp:CV8015@Vout = 9V， Start up with 1.1A load

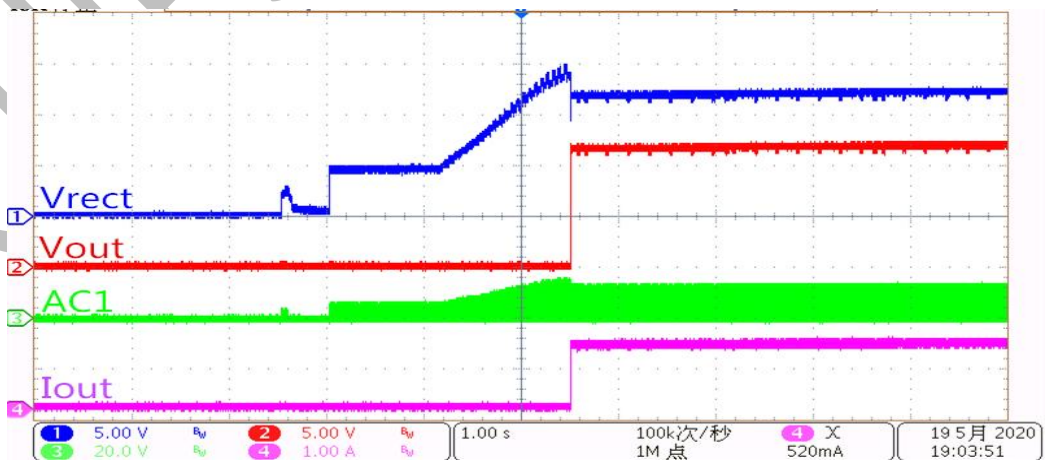


Figure 8. Transient Resp:CV8015@Vout = 12V， Start up with 1.25A load

7.3 OVP protection

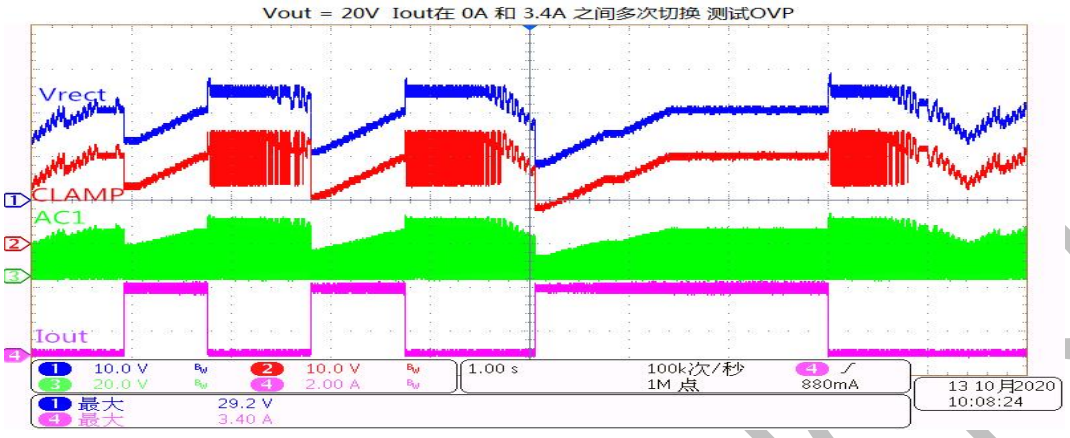


Figure 10. CV8015@Vout = 20V，3.4A to 0A load for testing OVP

7.4 OCP protection

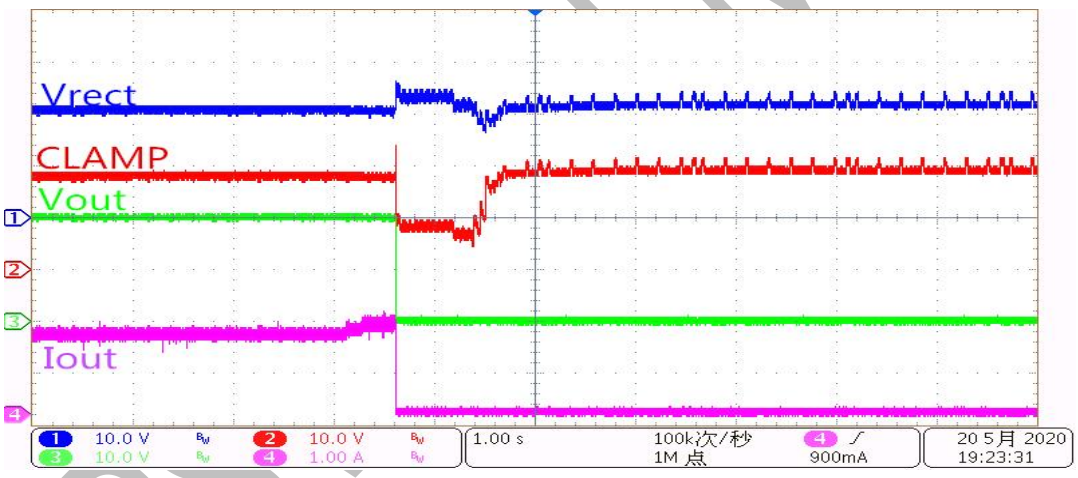


Figure 11. CV8015@Vout = 20V，OCP @load = 1.7A

8 Application circuit

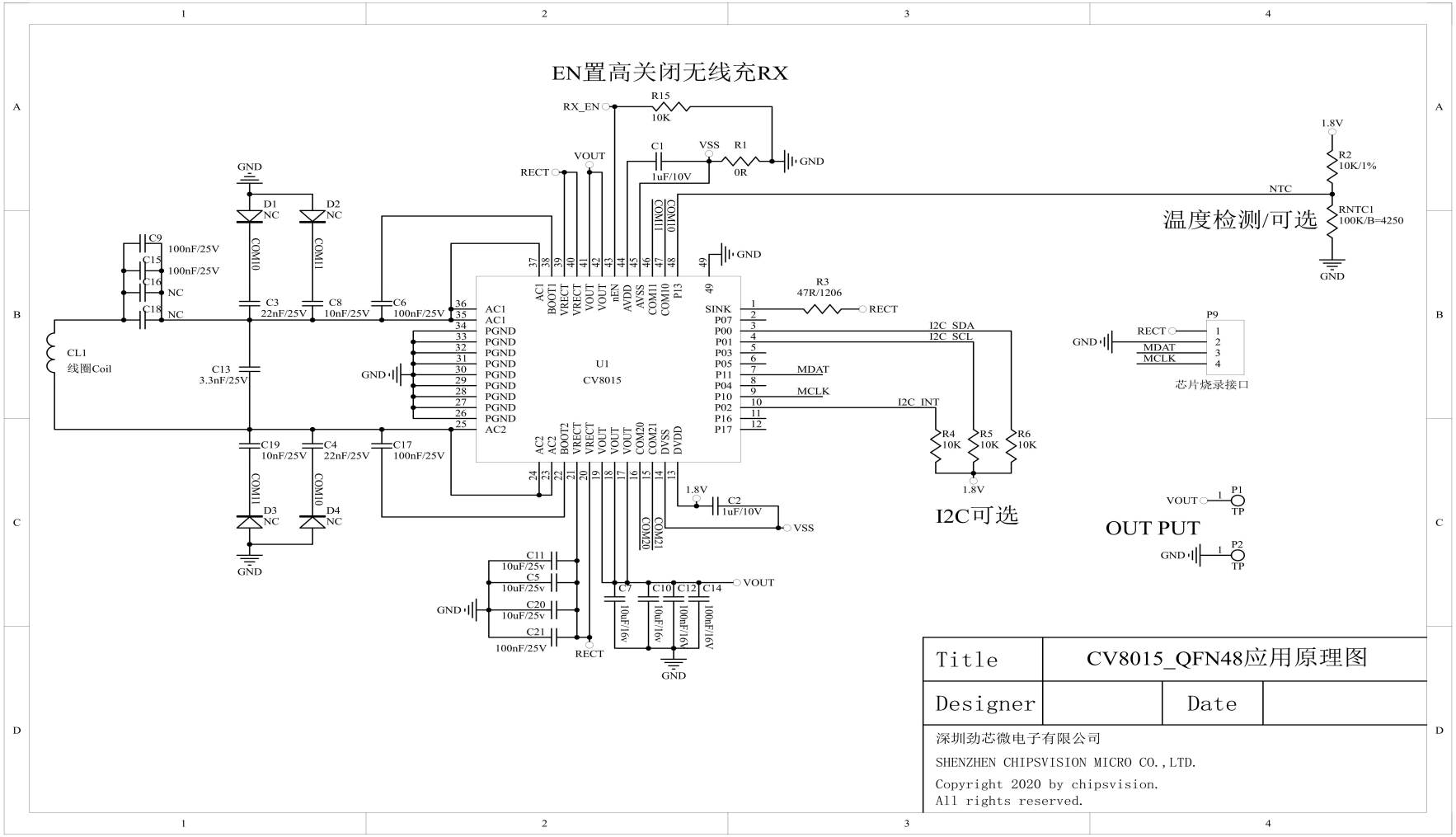
The circuit reference design is on page 17 of this document.

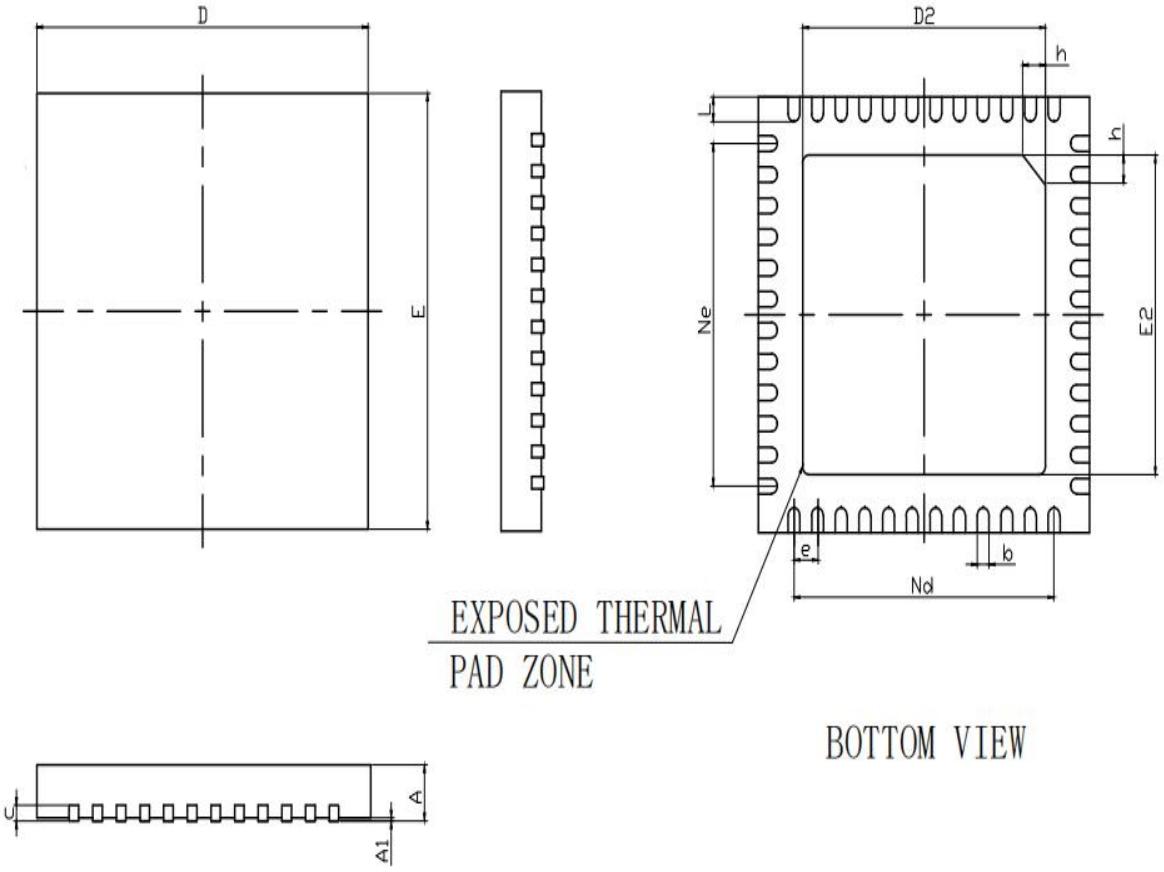
9 Package info

The package outline drawings are appended at the end of this document.

10 Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Shipping Packaging	Ambient Temperature
CV8015	QFN48 6.0 X 6.0 mm X 0.75mm	MSL3	Tape and reel	0°C to +85°C


EN置高关闭无线充RX
RX_EN
R15
10K
VOUT
RECT
C1
1uF/10V
VSS
R1
0R
GND
1.8V
R2
10K/1%
NTC
RNTC1
100K/B=4250
温度检测/可选
D1
NC
D2
NC
C9
100nF/25V
C15
100nF/25V
C16
NC
C18
NC
C3
22nF/25V
C8
10nF/25V
C6
100nF/25V
CL1
线圈Coil
C13
3.3nF/25V
U1
CV8015
AC1
PGND
AC2
SINK
P07
P00
P01
P03
P05
P11
P04
P10
P02
P16
P17
R3
47R/1206
I2C_SDA
I2C_SCL
MDAT
MCLK
I2C_INT
R4
10K
R5
10K
R6
10K
I2C可选
P9
芯片烧录接口
C19
10nF/25V
C4
22nF/25V
C17
100nF/25V
D3
NC
D4
NC
C2
1uF/10V
C11
10uF/25v
C5
10uF/25v
C20
10uF/25v
C21
100nF/25V
C7
10uF/16v
C10
10uF/16v
C12
100nF/16V
C14
100nF/16V
P1
TP
OUT PUT
P2
TP
Title
CV8015_QFN48应用原理图
Designer
Date
深圳劲芯微电子有限公司
SHENZHEN CHIPSVISION MICRO CO.,LTD.
Copyright 2020 by chipsvision.
All rights reserved.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.3REF		
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.3REF		
L	0.35	0.40	0.45
h	0.35REF		