1. Description

CV6056 is a System-on-Chip (SoC) that integrates a USB-C port, battery charge/discharge controller, and wireless charging control circuit. It enables a single-chip solution for single USB-C port, single cell battery magnetic power bank products, significantly saving system cost and board space. Both the battery charge/discharge and wireless charging control circuits integrate pre-drivers capable of directly driving MOSFETs. This structure ensures high system efficiency while allowing flexible layout for optimal PCBA thermal dissipation. The USB-C port supports various input/output fast charging protocols such as PPS/PD/SCP/FCP/QC/AFC/BC1.2. It features a built-in boost synchronous buck-boost controller, managing charging and discharging for a single-cell lithium battery. It also integrates wireless charging control circuits and pre-drivers, built-in Q-factor detection, communication decoding circuits, FOD detection, and supports Qi protocols including 5W (BPP), Apple Magnetic 7.5W, EPP 15W, Qi2.0, Qi2.2, etc.

CV6056 offers high integration, rich I/O interfaces, multiple high-precision ADCs, I2C Master and Slave interfaces, and two built-in SPI interfaces, supporting external SPI Flash and TFT image display functions.

CV6056 features low-power design, wide chip operating voltage range (2.8V ~ 5.5V), and USB-C port bidirectional automatic wake-up detection, ensuring extremely low system quiescent power consumption when implementing a wireless charging power bank system with a single chip. Supports Qi value wake-up for wireless charging.

2. Typical Applications

☆ Qi2.0 & Qi2.2 Magnetic Wireless Charging Power Bank

3. Features

- Chip operating voltage 2.8 ~ 5.5V;
- Standby power consumption <28uA @ 3.7V
- Built-in 32-bit processor, maximum frequency support 48MHz
- 31 channels 12-bit high-precision ADC
- Built-in boost synchronous buck-boost controller
- Built-in complete wireless charging circuit
  - Q-factor detection
  - Current/voltage decoding
  - High-speed PWM control circuit including dead-time control, PWM adjustment, phase-shift control
  - Inverter bridge driver circuit, resonant capacitor switching high-voltage driver circuit
  - FOD detection and OCP, OVP, OTP functions
- Built-in master/slave I2C interface, UART for system cascade expansion
- Built-in 2 SPI interfaces, supporting SPI Flash and image display
- Built-in DRP bidirectional full-featured Type-C port controller:
  - Supports PD2.0/PD3.0/PD3.1/PD3.2 PPS
  - Supports CC1/CC2/DP bidirectional low-power wake-up or GPIO wake-up
  - Supports fast charge and fast discharge functions
- Supports multiple fast charging protocol specifications
  - PD2.0/PD3.0/PD3.1/PD3.2(source/sink),(include Programmable Power Supply PPS）；

  Programmable Type-C pull-up resistor/pull-down resistor; built-in VCONN power supply and switch,coordinate E-marker function

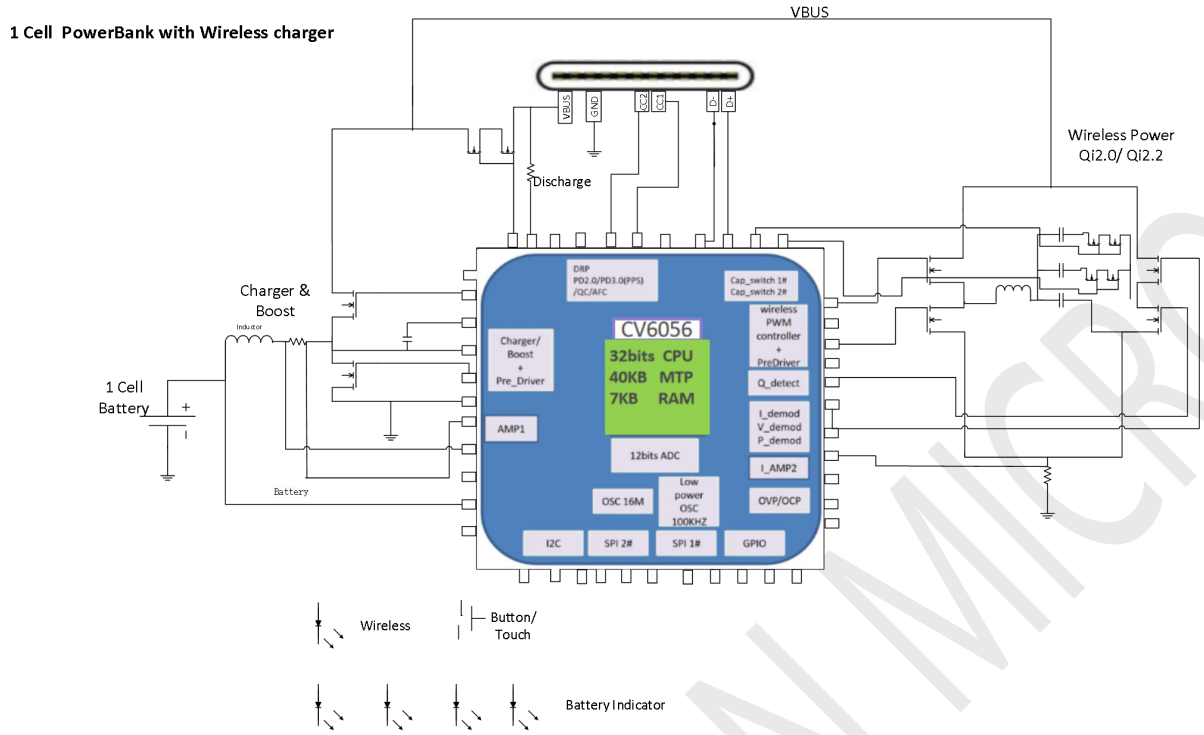
- Supports QC4.0+/QC3.0/QC2.0
- Supports AFC
- Supports FCP
- Supports SCP
- Compatible with BC1.2
- Supports line impedance compensation

- Charging Specifications
  - Supports single-cell lithium battery charging/discharging
  - Input voltage: VBAT ~ 24V
- Discharging Specifications
  - Output voltage: VBAT ~ 24V
  - Output current up to 5A
  - Single port output power up to 30W
- Power Indicator
  - Supports percentage battery level display
  - Supports expandable LED display
  - Supports 188 digital tube display
  - Supports TFT, OLED graphic display
- Wake-up Methods
  - Supports button wake-up
  - Supports USB-C port insertion wake-up
  - Supports touch, Q-value wireless charging wake-up
- Multiple protection mechanisms, safe and reliable
  - Input under-voltage, over-voltage protection
  - Input, output over-current protection
  - Short circuit protection
  - Battery over-charge, over-discharge, over-current protection
  - IC over-temperature, NTC over-temperature protection
- System flexibility, BOM reduction

4.Product Information

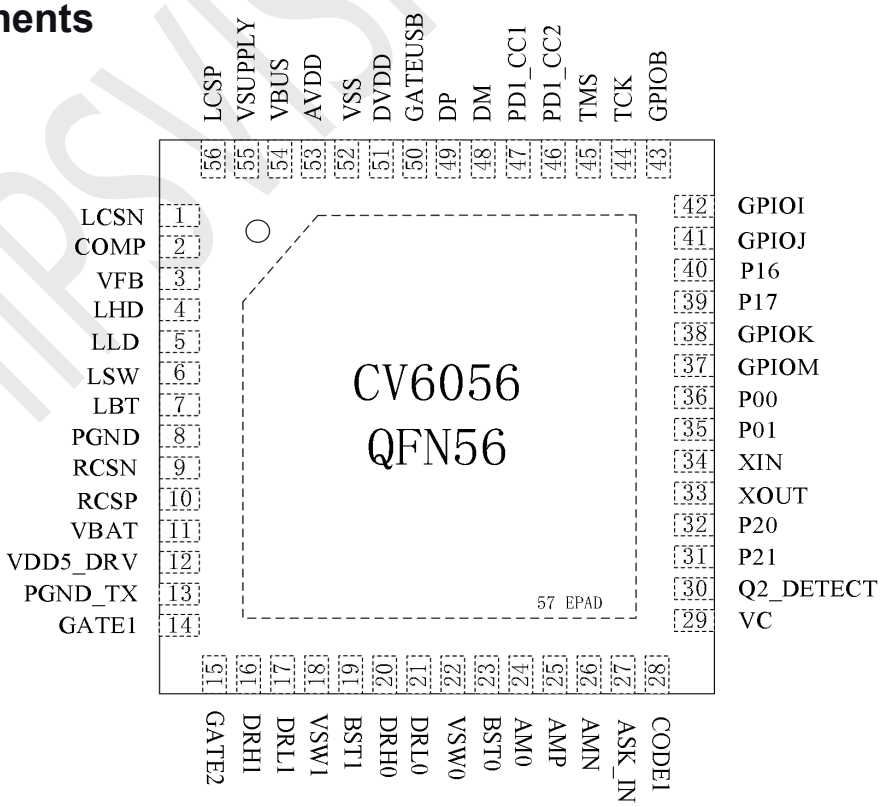
Product code	Package	Package Size
CV6056	QFN56	6.00 * 6.00 * 0.85 mm

5.Functional Block Diagram



6.Pin Assignments and Descriptions

6.1 Pin Assignments



6.2 Pin Descriptions

Pin Number	Pin Name	Description
1	LCSN	DCDC current sensing negative terminal
2	COMP	H-bridge compensation pin
3	VFB	H-bridge compensation pin
4	LHD	Buck-boost high-side MOSFET driver signal
5	LLD	Buck-boost low-side MOSFET driver signal
6	LSW	Buck-boost MOS source-drain inductor connection
7	LBT	Buck-boost high-side MOSFET output driver bias voltage
8	PGND	Power ground
9	RCSN	DCDC right-side current sensing negative pin
10	RCSP	DCDC right-side current sensing positive pin
11	VBAT	Battery voltage input pin
12	VDD5_DRV	Internal driver power supply
13	PGND_TX	Power ground
14	Gate1	Resonant capacitor switch MOSFET driver
15	Gate2	Resonant capacitor switch MOSFET driver
16	DRH1	Half-bridge high-voltage driver output pin 1
17	DRL1	Half-bridge low-voltage driver output pin 1
18	VSW1	Half-bridge high-voltage driver SW connection pin 1
19	BST1	Half-bridge high-voltage driver bootstrap pin 1
20	DRH0	Half-bridge high-voltage driver output pin 0
21	DRL0	Half-bridge low-voltage driver output pin 0
22	VSW0	Half-bridge high-voltage driver SW connection pin 0
23	BST0	Half-bridge high-voltage driver bootstrap pin 0

Pin Number	Pin Name	Description
24	AMO	Op-amp output pin
25	AMP	Op-amp non-inverting input pin
26	AMN	Op-amp inverting input pin
27	ASK_IN	Op-amp decoding input pin
28	CODE1	Current decoding input pin
29	VC	Over-voltage protection input
30	Q2_Detect	Q-factor detection input 2
31	P21	GPIO P21 pin
32	P20	GPIO P20 pin
33	XOUT	External crystal oscillator input pin
34	XIN	External crystal oscillator output pin
35	P01	General digital IO, outputs SPI1_MISO
36	P00	General digital IO, outputs SPI1_MOSI
37	GPIOM	Digital/Analog IO, outputs SPI1_CS
38	GPIOK/Uart_rx	Digital/Analog IO, outputs SPI1_SCK
39	P17/SDA	General digital IO, I2C, clock signal
40	P16/SCL	General digital IO, I2C, data signal
41	GPIOJ/INT2	Digital/Analog IO, external interrupt 2, SPI0_MISO
42	GPIOI/INT0	Digital/Analog IO, external interrupt 0,
43	GPIOB/INT1	Digital/Analog IO, external interrupt 1
44	TCK	Emulation/programming interface clock pin
45	TMS	Emulation/programming interface data pin
46	PD1_CC2	Type-C PD1_CC2 detection pin
47	PD1_CC1	Type-C PD1_CC1 detection pin
48	DM	Connect to USB port DM

Pin Number	Pin Name	Description
49	DP	Connect to USB port DP
50	Gateusb	USB port NMOS switch control, built-in boost driver
51	DVDD	Digital power supply pin 1.8V
52	VSS	Power ground
53	AVDD	5V power supply pin
54	VBUS	Vbus voltage sampling
55	Vsupply	Output voltage detection pin
56	LCSP	DCDC current sensing positive terminal
57	EPAD	Ground

7.Functional Description

7.1 CPU and Memory

Built-in 32-bit high-performance RISC architecture MCU, 48KB MTP program memory, 7KB SRAM data memory. Includes 64KHz low-frequency oscillator and 16MHz high-speed RC main clock oscillator. Built-in PLL circuit provides a 48MHz clock for the 32-bit CPU and up to 192MHz clock for the 16-bit high-speed PWM, ensuring the precision of frequency modulation, pulse width modulation, and phase shifting for wireless charging applications. Built-in watchdog circuit.

7.2 USB Type C and PD

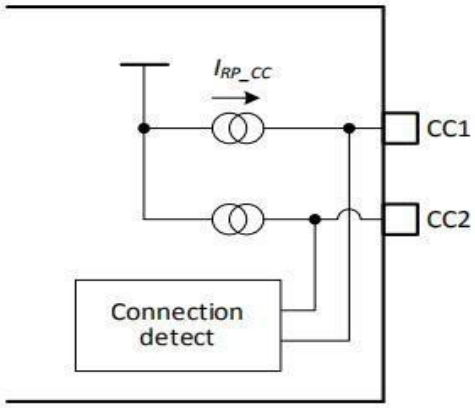
7.2.1 USB Type C Bus Termination and Detection

Type-C source pull-up resistor (Rp) is implemented by a configurable current source to advertise current capability. Attachment/detachment detection is done by multiple comparators with different threshold voltages to meet Type-C specifications. Built-in pull-down resistor (Rd) is configurable.

When Type-C acts as a sink, the pull-up resistor can be turned off and the pull-down resistor turned on. By default, Type-C enables the pull-down resistor upon power-up.

When Type-C acts as a source, the pull-up resistor is turned off, the pull-up resistor enable is turned on, and the corresponding current capability is configured.

When Type-C acts in DRP mode, the sink/source role is determined by toggling the pull-up/pull-down resistors and sampling the CC1/CC2 voltage levels. After entering low-power mode, Type-C automatically detects device insertion and wakes up the MCU.



7.2.1

7.2.2 VCONN

VCONN supplies power to E-marked cables via an internal MOSFET switch from the VDD output, with a maximum output power of 100mW. The VCONN switch is controlled by the on-chip MCU and can be turned off after reading the E-marked cable to reduce power consumption.

7.2.3 USB BC1.2, QC3.0, QC4.0

The chip supports USB Battery Charging Specification Revision 1.2 and High Voltage Dedicated Charging Port (HVDCP) QC3.0. HVDCP uses USB BC1.2 compatible signaling on D+ and D- to negotiate VBUS voltage requests. QC3.0 is backward compatible with Quick Charge 1.0 and 2.0. Quick Charge 3.0 offers finer voltage steps from 3.6V to 20V, in 200mV increments.

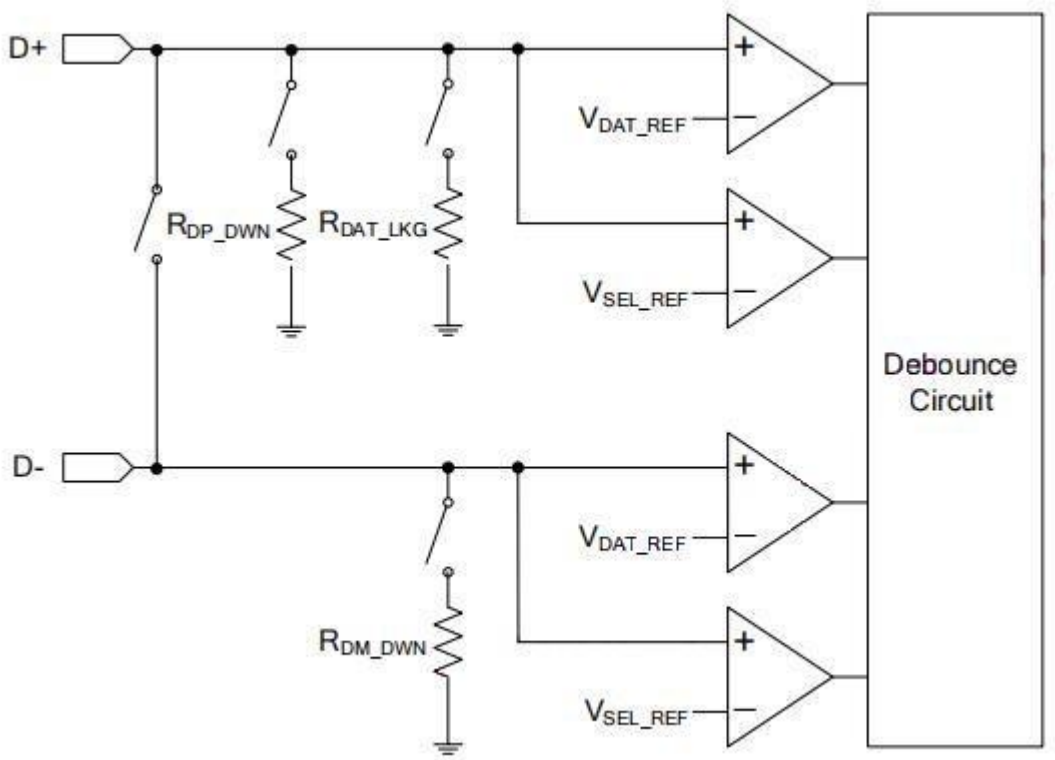


Figure 7.2.3 USB Interface D+, D- Internal Circuit Diagram

7.3 Boost Synchronous Charging and Discharging

7.3.1 Charging/Discharging Circuit Functional Description

CV6056 integrates a built-in battery charge/discharge hardware controller and MOSFET drivers. It supports peak current detection, a hardware triangular wave generator, configurable operating frequency from 200KHz to 800KHz, and input voltage feedforward. Comprehensive protection mechanisms include under-voltage lockout, over-voltage protection, over-current protection, short circuit protection and alert, and over-temperature protection. It supports a complete charging cycle management: trickle charging, constant current charging, and constant voltage charging. The battery full charge voltage is software configurable, supporting batteries with various voltages such as 4.2V, 4.35V, 4.4V, and 4.5V. Supports high-efficiency boost discharge mode with output voltage up to 24V.

7.4 Buck-Boost DC-DC Converter

7.4.1 Buck-Boost DC-DC Converter includes the following settings

- Configurable buck-boost and charge/discharge operating modes
- Adjustable output voltage from VBAT to 24V, 20mV per step
- High-side current sensing module for constant current/short circuit current protection
- Output over-voltage protection
- Supports software/resistor configurable operating frequency from 200kHz to 800kHz

- Configurable dead-time for driver module to control efficiency; configurable maximum and minimum voltages of the DC-DC control triangular wave to control output range.

7.5 Wireless Charging

7.5.1 H-Bridge Control PWM

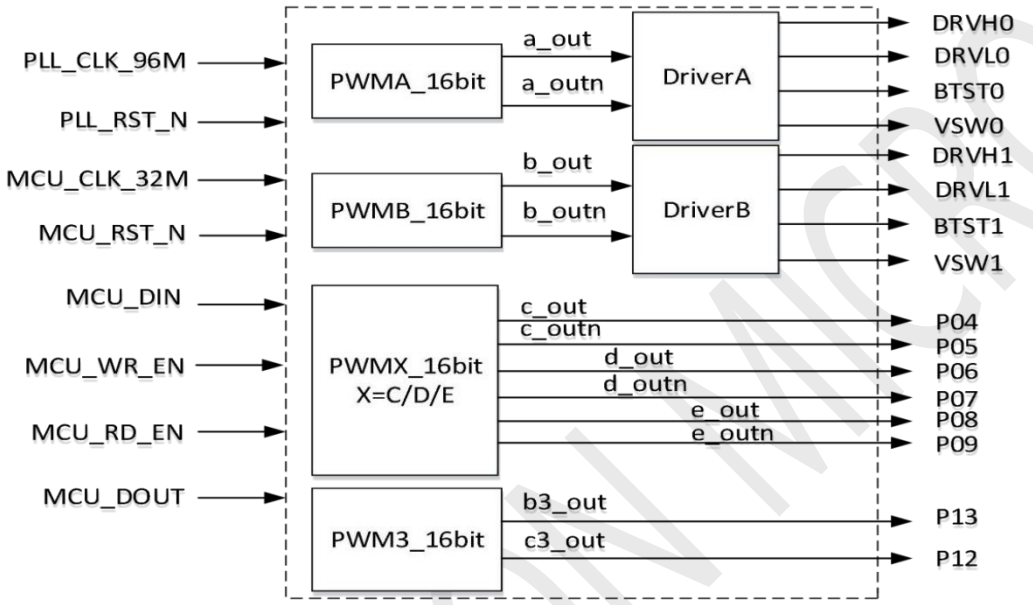


Figure 7.5.1 Full-Bridge Control PWM Diagram

PWM is designed with 128MHz frequency, integrating 5 PWM outputs consisting of A/B, C/D, E (i is used here to represent A/B/C/D/E), where ABC are complementary outputs, i_OUT/i_OUTN, D, E single-ended outputs. A/B channels integrate internal Driver A and Driver B.

Features:

- Each channel A/B, C/D, E has a 16-bit up-count auto-reload counter, 16-bit configurable period/duty cycle, and 8-bit dead-time register.
- Allows updating timer registers after a specified number of counter cycles (repeat counter).
- A/B, A/C, C/D can be combined into full-bridge, triple full-bridge outputs without mutual interference, each group stays synchronized, supports phase shifting, pulse width adjustment, dead-time. Note A/C can also be combined into full-bridge.
  - Where A/B forms a full-bridge, both share the period and duty cycle of channel A, use their own dead-time, channel B can phase shift based on channel A.
  - Where A/C forms a full-bridge, both share the period and duty cycle of channel A, use their own dead-time, channel C can phase shift based on channel A. The resources for channel C are reused from channel B, and channel C resources are multiplexed onto channel D, which can work independently.
  - Where C/D forms a full-bridge, both share the period and duty cycle of channel C, use their own dead-time, channel D can phase shift based on channel C.

- A/B/C can form 6 complementary PWM outputs,
  - Share A_COUNT, period of channel A;
  - Duty cycle, dead-time are used respectively;
  - Channel C resources are reused onto channel D;
- Brake input, supporting hardware brake and software brake;
  - Each i_OUT/i_OUTN has independent output enable control;
  - Supports online dynamic changes to period, duty cycle, dead-time, and 360-degree phase shift registers, ensuring period integrity.

PWM3_16BIT consists of two independent PWM outputs, B3_OUT/C3_OUT.

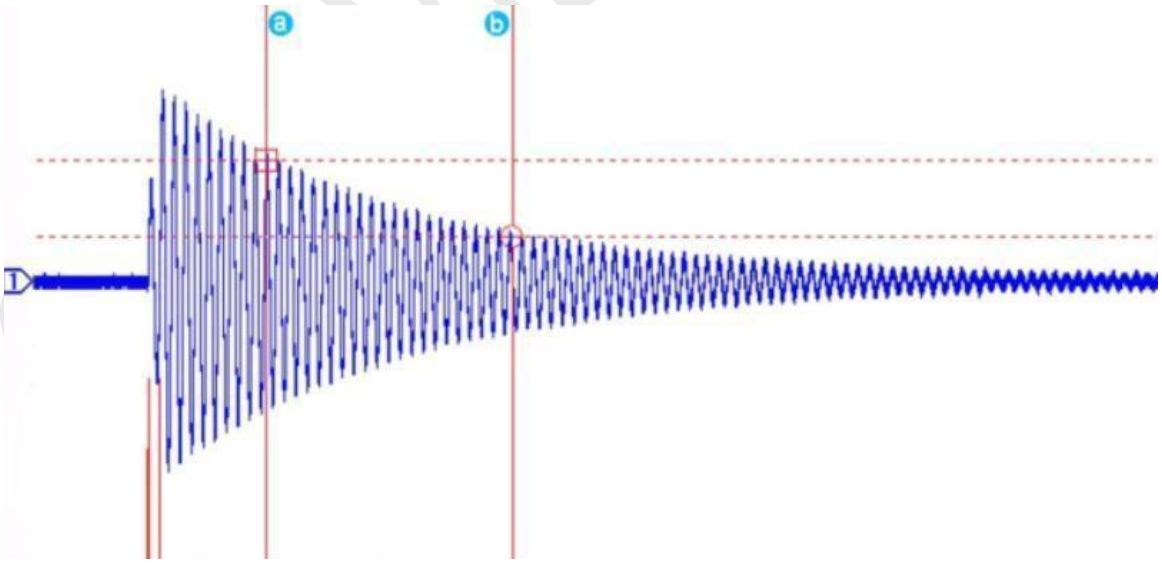
PWM3_16BIT has a 16-bit A_COUNT auto-reload counter.

Features:

- Basic timing;
- Supports driving 2 PWM waveforms simultaneously.

7.6 Q-factor Detection

Turn on the half-bridge high-side MOSFET to store energy in the LC circuit, then turn on the half-bridge low-side MOSFET. The LC circuit self-oscillates and discharges, forming a high-frequency, exponentially decaying oscillation as shown below:



7.7 Analog Ping

CV6056 sends a very short pulse to the LC circuit, causing it to oscillate. When an RX approaches, the oscillation amplitude of the LC circuit changes, thus detecting an RX. Analog ping significantly reduces the average standby power consumption of the TX.

7.8 Hardware Over-Voltage Protection

CV6056 integrates a built-in hardware over-voltage protection circuit. This enables fast trigger protection mechanism, preventing high voltage stress on transmitter system components and receiver devices due to abnormal conditions (e.g., foreign objects) causing excessively high coil resonant voltage. CV6056 features triple over-voltage protection. The first layer is software protection. When the VC voltage reaches or approaches the software preset protection voltage, the software stops increasing transmit power. When the VC voltage divided by R1/R2 exceeds the comparator N-terminal voltage (3.3V), the hardware protection mechanism triggers. The OVP signal generates a Half Bridge Lock signal, locking the full-bridge operating mode to half-bridge (Q3 off, Q4 normally on). At this point, Tx transmit power is halved, and an OVP interrupt is

generated. If the Tx receives normal communication signals from RX and the VC voltage no longer continues to rise, the software can decide whether to resume normal charging. If the VC voltage continues to rise under half-bridge mode, the system triggers the third level of protection, turning off Q1, Q3, and simultaneously turning on Q2, Q4 MOSFETs to enter a discharge state.

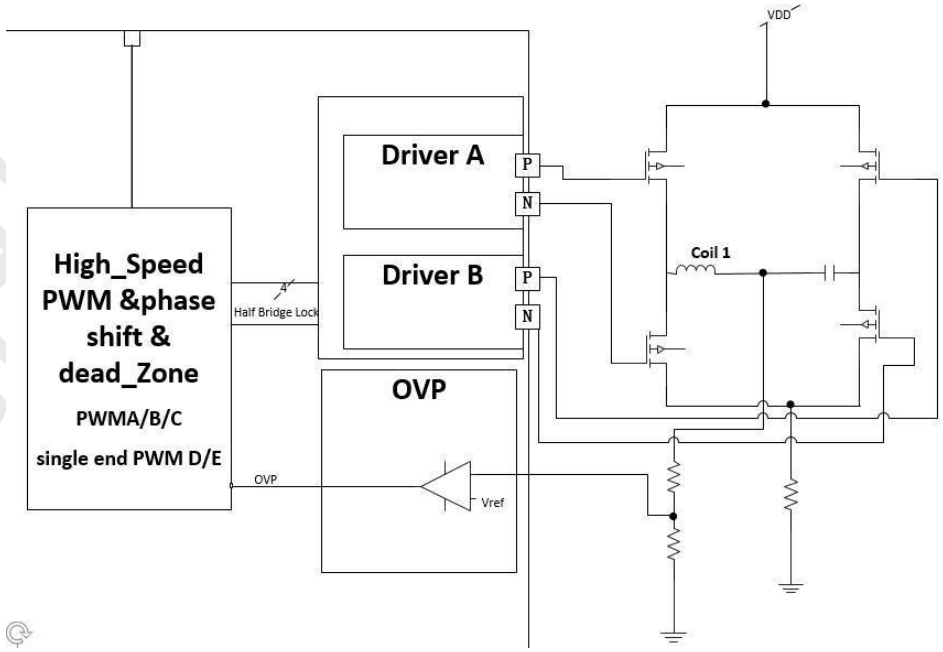


Figure 7.8.1 Hardware Protection Circuit Block Diagram

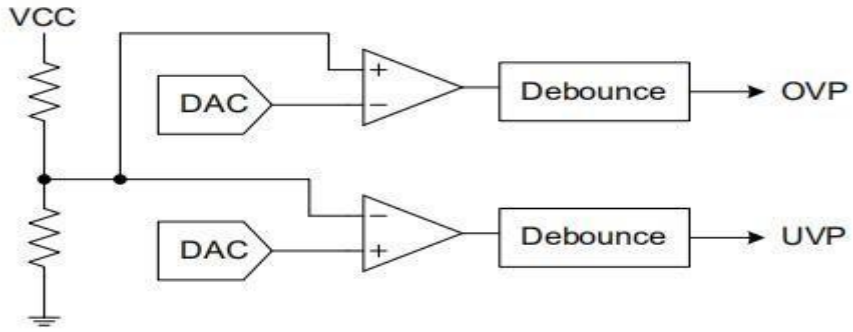
7.9 Foreign Object Detection (FOD) Function

CV6056 uses two methods, Q-factor and power loss, for foreign object detection, enabling fast and accurate judgment and protection: Q-factor detection: When the Q-factor detected by TX is lower than the preset value, a FOD alarm is quickly issued. Power loss: CV6056 features a high-precision ADC. When the TX power exceeds the power received by RX by more than a set value, TX makes an accurate judgment and triggers FOD protection. Current flowing through the wire causes a voltage drop due to the wire's resistance. To compensate for this drop, a compensation current source injects current into the VFB pin proportionally to the load current magnitude.

7.10 Protection Circuits

7.10.1 OVP and UVP

See Figure 7.10.1. The VCC voltage is compared with a reference voltage generated by a DAC to generate over-voltage and under-voltage signals. Simultaneously, the MCU is interrupted, and the external load switch control signal GATE is removed, turning off the load switch.



7.10.1

7.10.2 Over-Current Protection (OCP)

The load current signal is amplified by a current sense amplifier and then converted to data by an ADC. The over-current trigger point and de-bouncing time can be configured via firmware.

7.10.3 Over-Temperature Protection (OTP)

External over-temperature protection is implemented using a constant current source and a voltage comparator. The current source flows out of the pin and develops a voltage drop across an NTC thermistor. When this voltage drops below the internal reference voltage VOTP, the comparator output triggers an alarm, turns off the GATE signal, and generates an interrupt to the MCU. The voltage at the pin can also be measured using the ADC.

The NTC thermistor should be a 200kΩ or 100kΩ resistor with a B-value of 4100K. The over-temperature protection trigger point can be selected at 95°C, 105°C, 115°C, or 125°C.

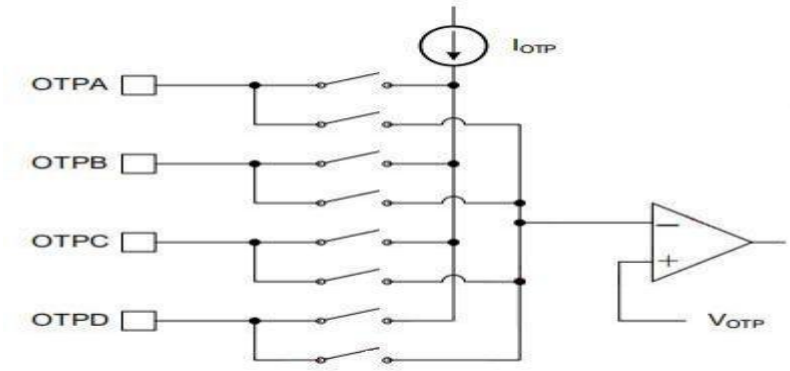


Figure 7.10.3 External Temperature Detection Component Schematic

7.15 Watchdog Timer

The watchdog timer can be used to detect CPU faults, such as software deadlocks caused by noise, voltage glitches, power loss, etc. When the internal counter of the watchdog timer overflows, a reset signal is generated to reset the CPU.

7.16 Reset

- The chip has the following reset signals:

- Power-On Reset (POR);
- 1.8V regulator output low reset;
- VCC supply under-voltage lockout (UVLO);
- VDD under-voltage reset;
- Watchdog timer reset;
- Program counter overflow reset.

8. Electrical Characteristics

8.1 Absolute Maximum Ratings (Based on ambient temperature 25℃)

Parameter	Symbol	Min	Max	Unit
Voltage Range	BST0, BST1, DRH0, DRH1, GATEUSB, GATE1, GATE2	-0.3	30	V
	PD1_CC1, PD1_CC2, VBAT, VBUS, RCSN, RCSP, VSW0, VSW1, Vsupply	-0.3	20	V
	DM, DP	-0.3	12	V
	DVDD	-0.3	2	V
	AVSS, PGND, PGND_TX	-0.3	0.3	V
	Other Pin	-0.3	6	V
Junction Temperature Range	T_J		125	℃
Storage Temperature Range	Tstg	-40	150	℃
Thermal Resistance (Junction to Ambient)	θ_{JA}	30		℃/W
Human Body Model (HBM)	ESD	-2000	2000	V

8.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	VCC, VBAT	2.8		20	V
I/O Voltage Range	PD1_CC1, PD1_CC2	0	5	5.5	V
Standby Power Consumption	Istandby			28	uA
Operating Temperature Range	T_A	-40		85	℃

8.3 DC Characteristics (Vcc=20V, Operating Temperature -20°C to +105°C)

8.3.1 Power Supply (Vcc, Vdd)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Supply Voltage	VCC		3		30	V
VCC Current, Normal Operation	ICC_OPR1	VCC ≥ 4.5V, No load on output, MCU frequency 10MHz				mA

Parameter	Symbol	Condition	Min	Typical	Max	Unit
VCC Current, Normal Operation	ICC_OPR2	VCC < 4.5V, No load on output, MCU frequency 10MHz				mA
Standby Current, MCU halted	ICC_STDBY	CC1 or CC2 floating				mA
		CC1 or CC2 connected to 5.1k pull-down resistor				mA
VCC Under-Voltage Lockout	VUVLO	VCC rising			2.85	V
		VCC falling	2.6			V
Built-in Regulator Output	VDD		4.75	5	5.25	V

8.3.2 Shunt Regulator

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Output Voltage Tolerance （Figure 8.3.2）	VOUT	VPWR=23V, Ta=25°C, 5V output			±1.5	%
		VPWR=23V, Ta=25°C, 3V ~ 21V output			±2.5	%
		VPWR=23V, Ta=-20°C ~ 105°C, 3V ~ 21V output			±3.5	%
PPS Voltage Step	Vpps_step	R_SENSE_=5mΩ, Av=80		20		mV
PPS Current Limit Step	Ipps_step	R_SENSE_=5mΩ, Av=80		50		mA
Current Limit Tolerance	ΔIPPS_CL	1A ≤ Current Limit ≤ 3A			±150	mA
		Current Limit > 3A			±5	%

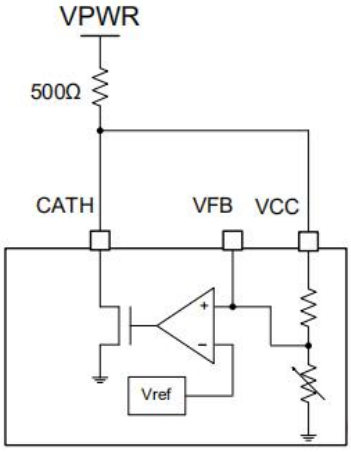


Figure 8.3.2 Shunt Regulator Test Circuit

8.3.3 Over-Voltage and Under-Voltage Protection (OVP, UVLO)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Under-Voltage Trigger Point	UVLO				3	V
OVP Step	VOVP_STEP			0.1		V
OVP Trigger Point Error	ΔVOVP				±5	%
UVP Voltage Trigger Point	VUVP			35		V
UVP Step	VUVP_STEP			0.1		V
UVP Trigger Point Error	ΔVUVP				±5	%

8.3.4 Over-Current Protection (OCP)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
OCP Trigger Point	IOCP	Rs = 5mΩ, Av = 80	0.5		6.4	A
OCP Step	ΔIOCP	Rs = 5mΩ, Av = 80, IOCP=3.6A		0.1		A

8.3.5 ADC

Parameter	Symbol	Condition	Min	Typical	Max	Unit
ADC Resolution	NADC			12		bit
ADC INL	INLADC	Ta = 25℃, Vin = 2.5V			±5	LSB
ADC DNL	DNLADC	Ta = 25℃, Vin = 2.5V			±5	LSB
ADC Reference Voltage	VREF_ADC	Selectable 2.56V/4.3V, Ta=25℃, VCC=5V		2.56		V
				4.3		V

8.3.6 CC1, CC2

Parameter	Symbol	Condition	Min	Typical	Max	Unit
BMC Transmit Output High Level	VOH_CC		1.05	1.125	1.2	V
BMC Transmit Output Low Level	VOL_CC				0.075	V
BMC Receive Input High Level	VIH_CC		0.67		1.45	V
BMC Receive Input Low Level	VIL_CC		-0.25		0.43	V
BMC Transmit Output Impedance	ZDriver_CC		33		75	Ω

Parameter	Symbol	Condition	Min	Typical	Max	Unit
BMC Receive Input Impedance	ZBMCRX_CC		1			MΩ
CC1, CC2 Pull-up Current	IRP_CC	0.5A current @5V		80		μA
		1.5A current @5V		180		μA
		3.0A current @5V		330		μA
CC1, CC2 Insertion Detection Level	VRd_CC	0.5A current @5V		1.6		V
		1.5A current @5V		1.6		V
		3.0A current @5V		2.6		V

8.3.7 VCONN

Parameter	Symbol	Condition	Min	Typical	Max	Unit
VCONN Voltage	VCONN	VCC = 5V, IVCONN = 0mA		4.85		V
		VCC = 5V, IVCONN = 30mA		3.39		V

8.3.8 USB Port D+, D- Pins

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Data Detect Voltage	VDAT_REF		0.25	0.35	0.4	V
Output Select Voltage	VSEL_REF		1.8			V
D+/D- Pull-down Resistor	RDWN		14.25		24.8	kΩ
Resistance between D+, D- in DCP mode	RDCP_DAT			30	40	Ω

8.3.9 External Temperature Detection

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Over-Temperature Detection Current Source	IOTP			20.5		μA

8.3.10 On-Chip Temperature Detection

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Internal Temperature Detection Accuracy	TTS				±10	℃

8.3.11 GPIO

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Output Low Level	VOL_GPIO10m	IOL = 10mA, VDD = 5V; VFB, GPIOB, GPIOM-K, P16, P17			0.5	V
GPIO Output High-Z Leakage	IZ_GPIO				10	μA
Input High Level (VTHS=0)	VIH	VFB, GPIOB, GPIOM-K, P16, P17	0.8*VDD		VDD	V
Input Low Level (VTHS=0)	VIL	VFB, GPIOB, GPIOM-K, P16, P17	0		0.2*VDD	V
Input High Level (VTHS=1)	VIH	VFB, GPIOB, GPIOM-K, P16, P17	0.52*VDD		VDD	V
Input Low Level (VTHS=1)	VIL	VFB, GPIOB, GPIOM-K, P16, P17	0		0.13*VDD	V

8.3.12 DC-DC Buck-Boost Converter

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Output Level	Vout_sel	Iout = 1mA	3.2		34	V
Over-Voltage Upper Limit	Ovp_rise	Vout > % of ideal value, trigger OVP	112.5		120	%
Over-Voltage Lower Limit	Ovp_fall	Vout < % of ideal value, recover	90		100	%

8.4 AC Signal Characteristics (Vcc=20V, Temperature -20°C to +105°C)

8.4.1 Internal Oscillator

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Main Oscillator Frequency	Foscm			16		MHz
Low Frequency Clock Oscillator Frequency	Fosca			64		KHz

8.4.2 USB-PD BMC Transmit and Receive

Parameter	Symbol	Condition	Min	Typical	Max	Unit
BMC Data Rate	f_BMC_		270	300	330	KHz
BMC Signal Rise Time	t_RISE_BMC_				300	ns

Parameter	Symbol	Condition	Min	Typical	Max	Unit
BMC Signal Fall Time	t_FALL_BMC_				300	ns
Time from last rising edge to driving termination	t_HOLD_BMC_				1	μs
Time from last data bit to first data bit of next packet	t_IFG_BMC_				25	μs
Time from last data bit to driving termination	t_END_EMC_				23	μs
BMC Receive Bandwidth Limiting Window	t_RXFTR_BMC_				100	ns
Time window to detect non-idle state	t_NIDLE_BMC_	12		20	μs	
Level transitions required to exit idle state	N_NIDLE_BMC_	3				
BMC Transmit "1" Pulse Width	t_PULSE1_BMC_	Ta = 25℃, CC total capacitance = 1010pF, CC pin series resistor = 47Ω	1.4		1.8	

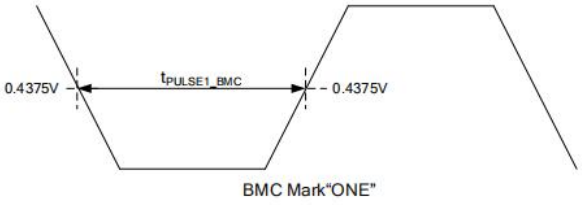


Figure 8.4.2a BMC Timing Diagram

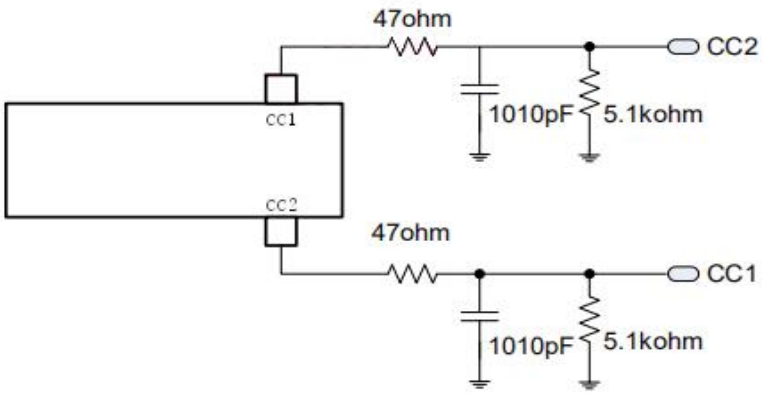


Figure 8.4.2b Test Circuit for BMC Transmit "1" Signal Pulse Width

8.4.3 DC-DC Buck-Boost Converter

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Control Frequency	fdcdc		190	390	755	KHz
Driver Dead Time	Driver_dt		39		140	ns
Debounce Delay	debounce		100		200	ns

9. Application Schematic

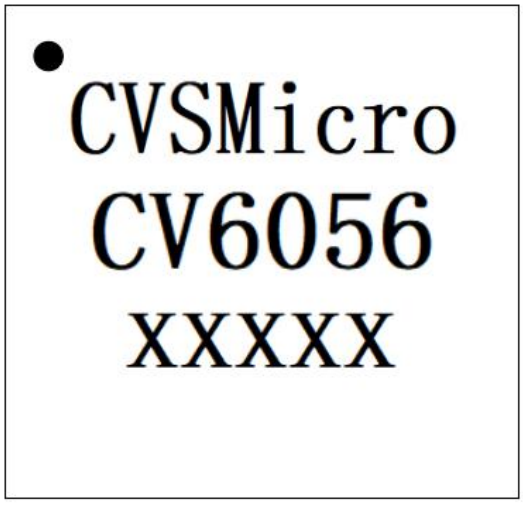
Refer to page 22 for CV6056 product application schematic.

10. Package Information

Refer to page 21 for package outline drawing.

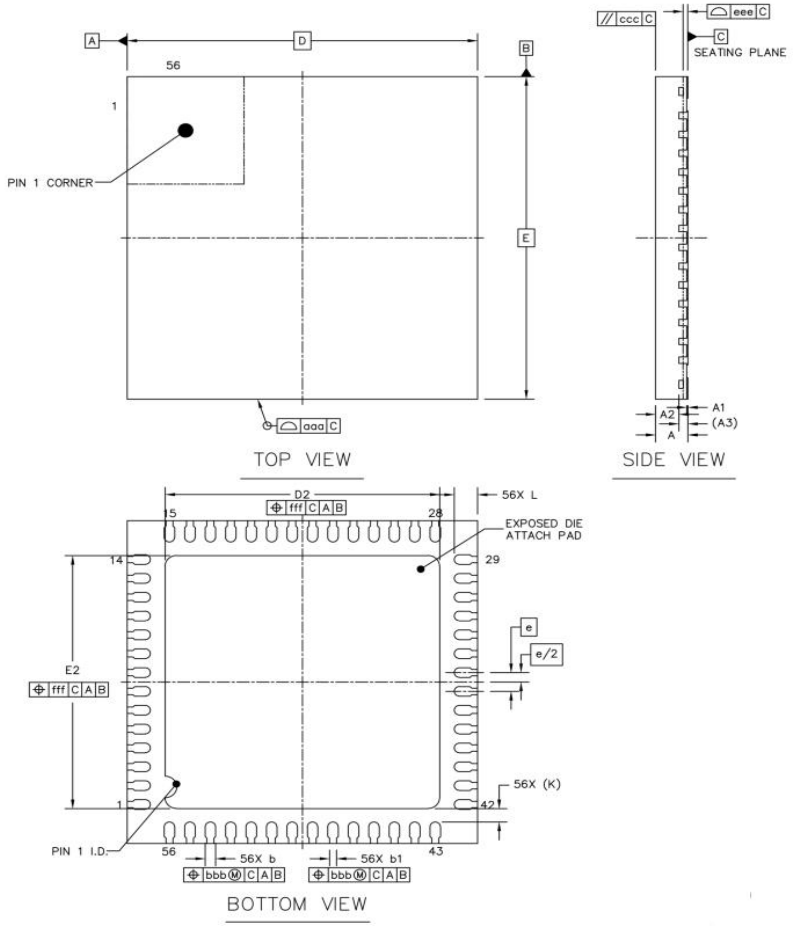
Product Number	Package	MSL	Packaging	MPQ
CV6056	QFN56 (6.00 * 6.00 * 0.85 mm)	Level 3	Reel	3000 PCS

11. Marking Diagram



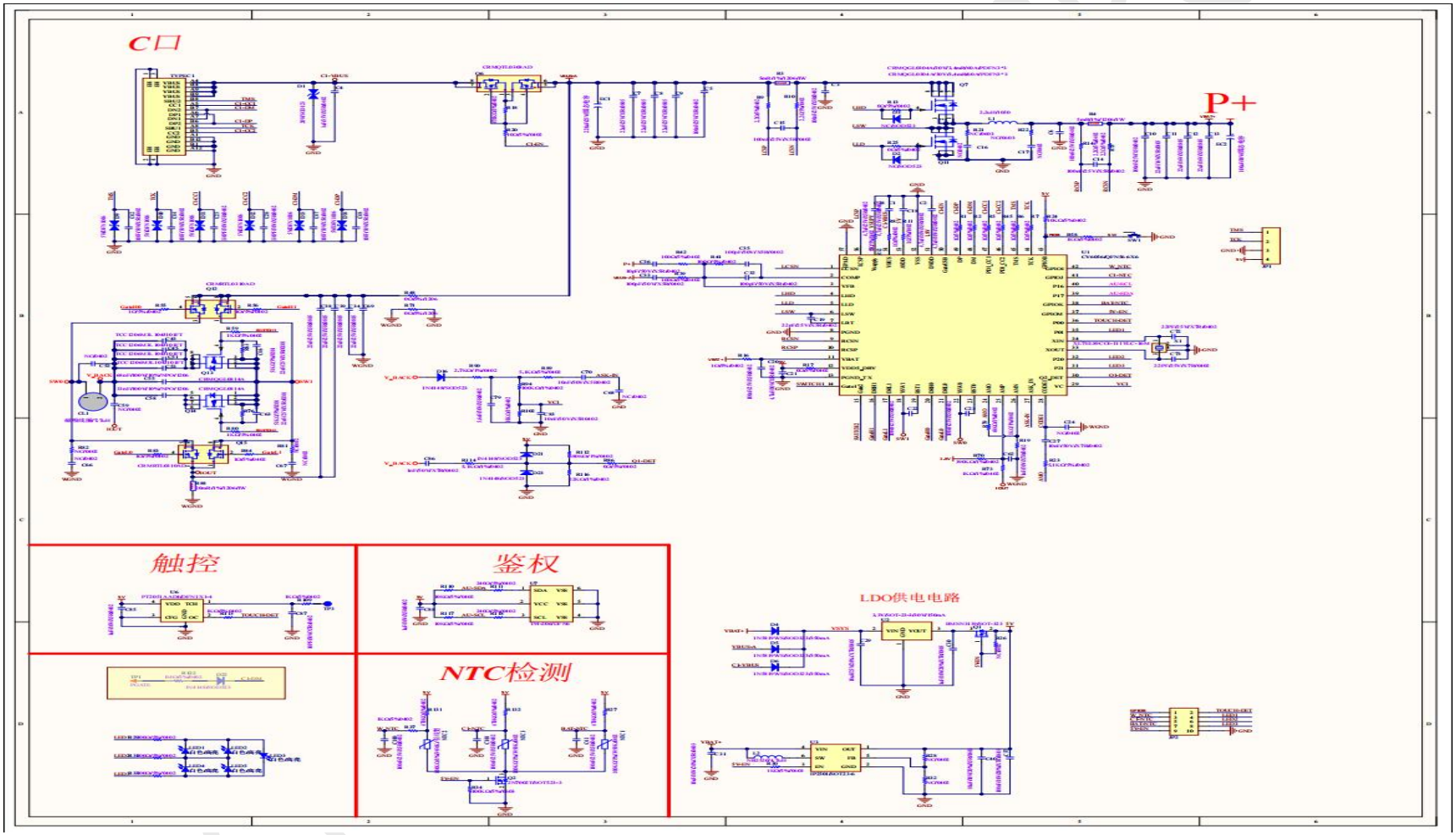
Location	Marking Content	Meaning
Line 1	CVSMicro	Company name
Line 2	CV6056	The Part Number
Line 3	XXXXX	Lot Number

12.Package Outline Drawing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	-	0.02	0.05
A2	-	0.4	-
A3	0.152REF		
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
D	5.9	6	6.1
E	5.9	6	6.1
D2	4.6	4.7	4.8
E2	4.6	4.7	4.8
e	0.35BSC		
L	0.30	0.40	0.5
K	0.25REF		

12. Application Schematic



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