Wireless Power Transmitter for Smartphones with PD and 15W Application

1 Description

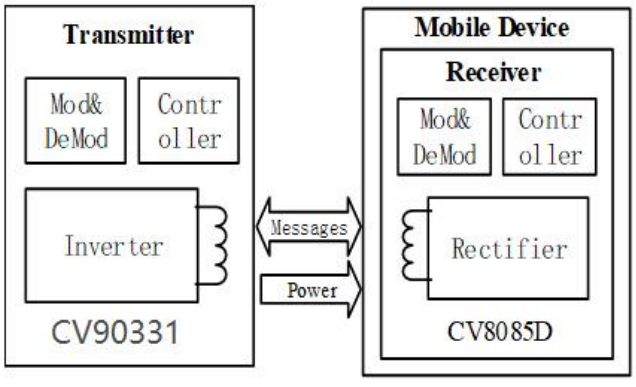
The CV90331 is a wireless power transmitter controller that integrates all required functions for the WPC "Qi" compliant wireless power transmitter design.which supports various adapters such as PD2.0, PD3.0, QC2.0, QC3.0, AFC and so on.Compliance with the latest WPC V1.2 standard, support MP-A11 coil,support customer coil customized solution, support BPP 5W, Apple 7.5W, Samsung 10W, EPP 15W charging.

The CV90331 has Integrated over voltage protection, over current protection, over temperature protection and other functions, and supports FOD detection.

The CV90331 is a QFN48 package, and integrates full bridge drive circuit and voltage & current communication decoding function module, which can significantly reduce PCB size and BOM cost.

2 Typical Applications

☆ BPP and EPP wireless charging pads
☆ Android fast charging pads
☆ Tablets
☆ Up to 7.5W charging for iPhones



3 Features

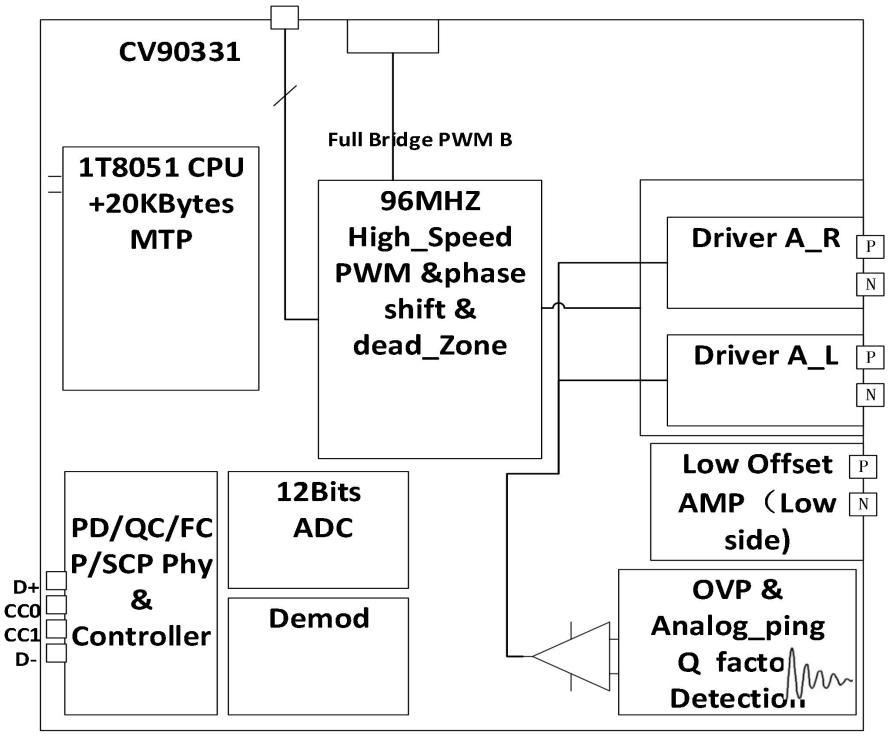
- WPC 1.2.4 compatible
- Power transfer up to 15W in EPP mode
- 16kB Multiple-time programmable (MTP) non-volatile memory for expanded feature support
- support 2 equipment wireless charging at the same time
- Integrated drivers for external power MOSFETs
- Real-time foreign object detection (FOD)
- Over voltage、over temperature and over current protection
- Supports I2C interface
- Integrated voltage and current sense amplifier
- LED for system status indication
- Ambient operating temperature: -40℃ to 85℃

4 Product Information

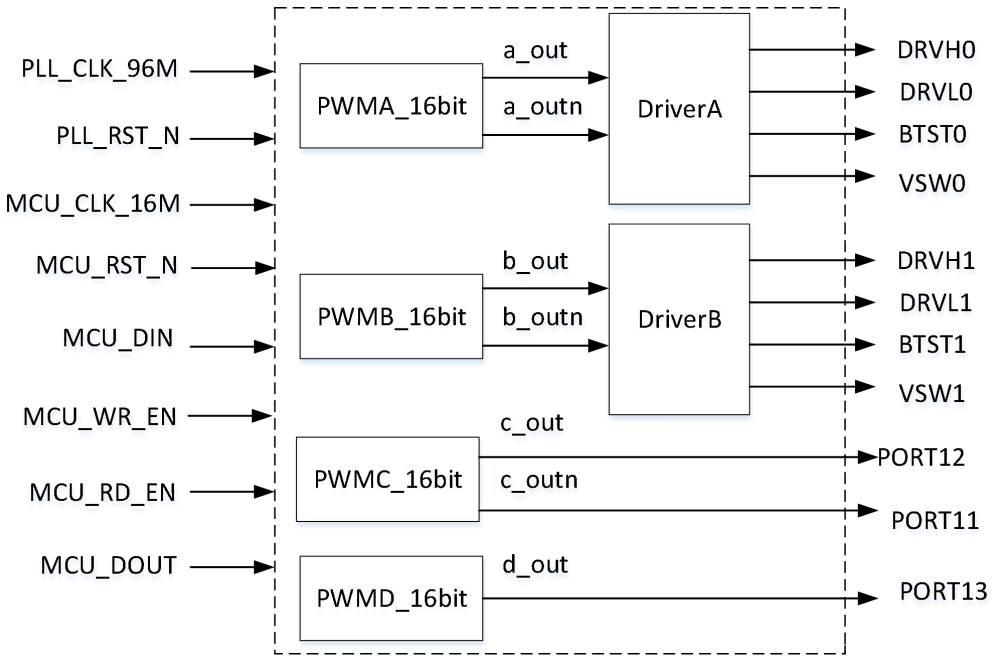
Orderable Part Number	Package Type	Package Size
CV90331	QFN48	6.00 * 6.00 * 0.75 mm

1. Function block diagram

1.1 Chip Block diagram

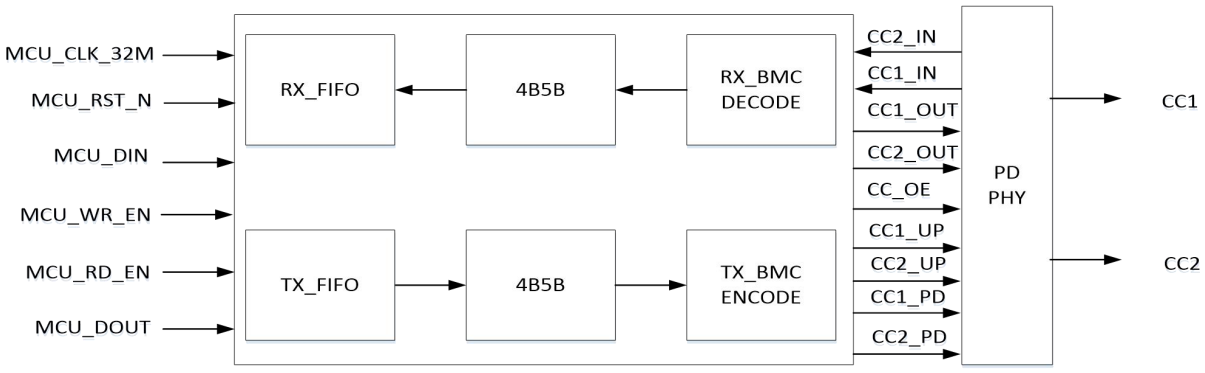


1.2 PWM generator Architecture



PWM A&B with the MOS can driver a full bridge inverter, PWM C and external power stage to compose another full bridge driver to drive one coils, the single end PWMD is a controller for voltage regulating solution.

1.3 Type_C/PD interface



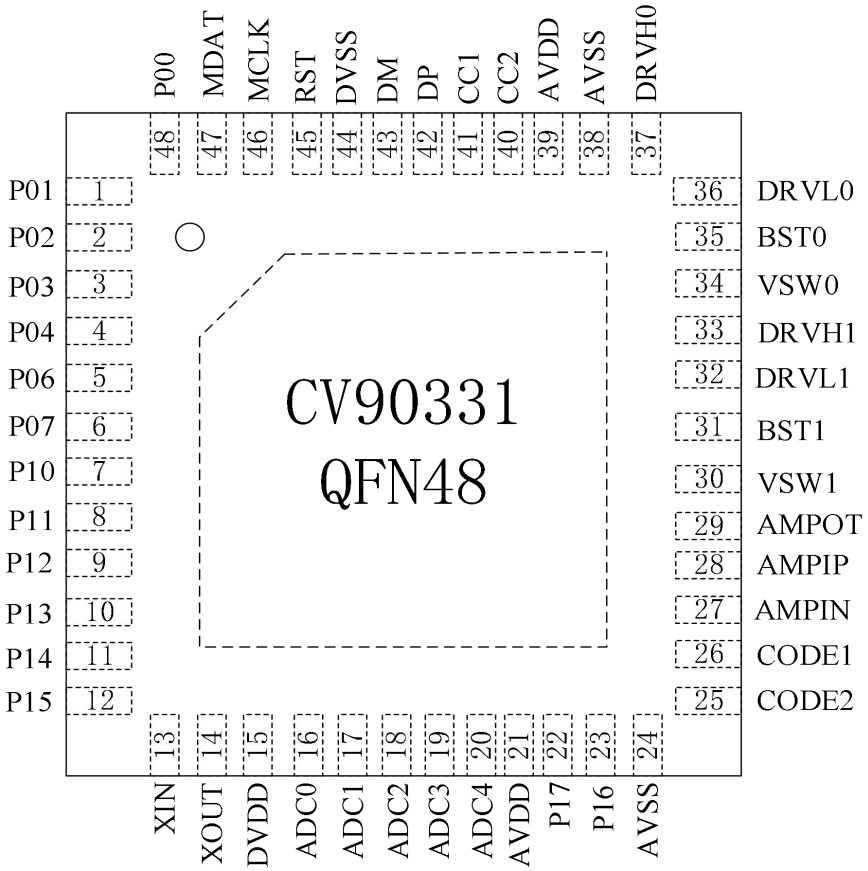
PD interface include Phy layer 、Link layer and codes controller and contact to CPU bus through FIFO, this PD interface work as sink mode , support PD 2.0/3.0 standards.

1.4 QC D+/D- interface

Built in QC D+/D- interface to support USB_ BC1.2 SDP/CDP/DCP/AFC/FCP/SCP power supply devices , the D+/D- voltage level as following table。

D+	D-	Output Voltage
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	Continuous mode
0.6V	High-Z	5V (Default)

2. Pin Assignment



Pin Descriptions:

Pin No.	Name	Description
1	P01	General-purpose digital I/O pin External interrupt PIN
2	P02	General-purpose digital I/O pin Serial 0 transmit data
3	P03	General-purpose digital I/O pin Serial 0 receive data
4	P04	General-purpose digital I/O pin
5	P06	General-purpose digital I/O pin
6	P07	General-purpose digital I/O pin
7	P10	General-purpose digital I/O pin Timer 0 external input
8	P11	General-purpose digital I/O pin Timer 1 external input PWMC highend output pin
9	P12	General-purpose digital I/O pin Timer 2 external input PWMC Lowend output pin

10	P13	General-purpose digital I/O pin Count/Capture 0 PWMD single end PWM output for voltage regulating control
11	P14	General-purpose digital I/O pin Count/Capture 1
12	P15	General-purpose digital I/O pin Serial 1 transmit data
13	Xin	External crystal pin
14	Xout	External crystal pin
15	DVDD	VDD1.8V
16	ADC0	ADC input channel 0
17	ADC1	ADC input channel 1
18	ADC2	ADC input channel 2
19	ADC3	ADC input channel 3
20	ADC4	ADC input channel 4
21	AVDD	Power source
22	P17	General-purpose digital I/O pin I2C SDA ADC
23	P16	General-purpose digital I/O pin I2C SCL ADC
24	VSS	GND
25	CODE2	Current sensing demodulation input
26	CODE1	Voltage sensing demodulation input
27	AMPIN	Op-amp nagtive input terminal
28	AMPIP	Op-amp postive input terminal
29	AMPOUT	Op-amp output terminal
30	VSW1	MOSFET Half-Bridge Driver 1 High-side source connection.
31	BST1	MOSFET Half-Bridge Driver 1 High-side bootstrap supply
32	DRL1	MOSET Half-Bridge Driver 1 Low-Side output
33	DRH1	MOSET Half-Bridge Driver 1 High-Side output
34	VSW0	MOSFET Half-Bridge Driver 0 High-side source connection.
35	BST0	MOSFET Half-Bridge Driver 0 High-side bootstrap supply
36	DRL0	MOSFET Half-Bridge Driver 0 Low-Side output
37	DRH0	MOSFET Half-Bridge Driver 0 High-Side output
38	AVSS	Ground
39	AVDD	Supply voltage
40	CC2	Type_C PD interface
41	CC1	Type_C PD interface
42	DP	General-purpose digital I/O pin
43	DM	General-purpose digital I/O pin
44	AVSS	Ground
45	RST	Reset pin
46	MCLK	Emulation port clock pin
47	MDAT	Emulation port data pin
48	P00	General-purpose digital I/O pin External interrupt 0

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed in Table 2 and Table 3 can cause permanent damage to the CV90331. Functional operation of the CV90331 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability.

3.1 Absolute Maximum Ratings

Note: All voltages are referenced to ground.

Symbol/Pins	Parameter	Conditions	Minimum	Maximum	Units
VSW1,VSW2	Absolute Maximum Pin Voltage		-0.3	20	V
BST0, BST1,DRH0, DRH1	Absolute Maximum Pin Voltage		-0.3	25	V
DRL0, DRL1,CC1, CC2,AMPIN,AMPIP,AMPOT, DP,DM,P00—P07,P10—P17,ADC0—ADC4, CODE1,CODE2,AVDD, nRST,XIN, XOUT,MDAT,MCLK	Absolute Maximum Pin Voltage		-0.3	6	V
AVSS、VSS	Absolute Maximum Pin Voltage		-0.3	0.3	V
DVDD	Absolute Maximum Pin Voltage		-0.3	2	V
HBM	ESD Rating - Human Body Model	All pins	-2000	2000	V

4. Thermal Characteristics

4.1 Thermal Characteristics

Symbol	Parameter	Value	Units
θ_{JA}	Thermal Resistance Junction to Ambient [a], [b], [c]	35.66	℃/W
θ_{JC}	Thermal Resistance Junction to Case [a], [b], [c]	26.8	℃/W
θ_{JB}	Thermal Resistance Junction to Board [a], [b], [c]	6.36	℃/W
T_J	Operating Junction Temperature	0 to +125	℃
T_{AMB}	Ambient Operating Temperature	0 to +85	℃
T_{STOR}	Storage Temperature	150	℃
T_{BUMP}	Maximum Soldering Temperature (Reflow, Pb-Free)	260	℃

[a] The maximum power dissipation is $P_{D\ (MAX)} = (T_{J\ (MAX)} - T_{AMB}) / \theta_{JA}$ where $T_{J\ (MAX)}$ is 125°C.

(See Table 4.) Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

[b] This thermal rating was calculated on a JEDEC 51 standard 4-layer board with the dimensions 3" x 4.5" in still air conditions.

[c] Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

5. Recommended Operating Conditions

5.1 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{IN}	Input Operating Range [a], [b]	4.5	5	5.5	V
V_{DVDD}	1.8V LDO output voltage	1.6	1.8	2	V

[a] The input voltage operating range is dependent upon the type of transmitter power stage (full-bridge, half-bridge) and transmitting coil inductance. WPC specifications should be consulted for appropriate input voltage ranges by end product type.

[b] The minimum for this specification is the minimum IC operating specification. Full power transfer will not occur at this level.

5.2 ESD information

Test Model	Pins	Ratings	Units
Human BodyModel（HBM）	All pins	+/- 2000	V
Charged-Device Model (CDM)	All pins	+/- 500	V

6. Electrical Characteristics

6.1 Electrical Characteristics

V_{IN} = 5V , Typical values are at 25°C, unless otherwise noted.

Note: See important notes at the end of the table.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Input Supplies						
V_{IN}	Input Operating Range		3.3	5	5.5	V
I_{IN}	Operating Mode Input Current	Normal power transfer state		10		mA
Analog to Digital Converter						
N	Resolution			12		Bit
Channel	Number of Channels			14		
$V_{IN,FS}$	Full Scale Input Voltage			VDD		V
Operational Amplifiers						

V_{IO}	Input offset voltatge	Vcc = 5V			5	mV
I_{IO}	Input offset current	Vo = 1.4V			80	nA
CMMR	Common-mode rejection ratio	V_{IC} = 5V, 25°C		70		dB
SR	Slew rate at unity gain	R_L = 1MΩ, C_L = 30pF		0.5	5	V/μS
B_I	Unity-gain bandwidth	R_L = 1MΩ, C_L = 20pF		1.2		MHz
V_n	Equivalent input nose voltage	R_s = 100Ω, V_i = 0V, f = 1kHz		35		nV/√Hz
LDO18 (C_{OUT}=1μF)						
V_{OUT18}	Output Voltage			1.8		V
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Accuracy			±5		%
I_{OUT18_MAX}	Maximum Output Load Current			10		mA
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Threshold Rising		140		°C
		Threshold Falling		120		°C
Clock Oscillators						
F_{RC-OSC}	Internal RC-OSC Clock Frequency		12	16	20	MHz
$F_{CRYSTAL}$	External Crystal Clock Frequency		12	20	24	MHz
F_{SYSCLK}	OSC Clock Frequency		12	16	24	MHz
$F_{PLL-OUT}$	Phase Lock-Loop (PLL) Voltage Controlled Oscillator (VCO) Frequency [d]		12	84	96	MHz

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
General Purpose Inputs/Outputs (GPIO)						
V_{IH}	Input HIGH Voltage		0.7 *VDD			V
V_{IL}	Input LOW Voltage				0.3 *VDD	V
I_{LKG}	Leakage Current		-1.0		1.0	μA
V_{OH}	Output Logic HIGH	VDD = 5.0V, I_{OH} = 8mA	4.3			V
V_{OL}	Output Logic LOW	VDD = 5.0V, I_{IH} = 8mA			0.7	V

6.2 Overview

The simplified block diagram of the CV90331 is shown in Figure 3 and contains the following functions:

- Optimized and compliant support of WPC and High-Speed-Charger transmitter protocols.
- Supports WPC low power transmitter types with external MOSFET.
- Embedded 8-bits enhanced 8051core, with 16kBytes NVRAM .
- Supports high speed serial flash (SPI interface) for system development, application development, and troubleshooting.
- Dithered pulse-width modulation (PWM) controller for high resolution voltage modulation.
- Multiple enhanced demodulation schemes using fewer external components for robust communication.
- Built-in SPI and URAT interface to communicate with external devices.
- Built-in PLL and clock synthesizer for PWM generation and back channel communication.
- Supports variable logic I/O voltages with dedicated VDD pin.
- Built-in general purpose 12-bit, 100ksps ADC for temperature, voltage, current measurement, and signal processing.
- Two banks of GPIOs with a dedicated power supply.

6.3 Overview of GPIO Usage

On the CV90331 transmitter IC, there are two banks of GPIOs, P0 and P1 ports, which can be configured for various functions. P1.6 and P1.7 are configurable as GPIO or ADCs input.

6.4 ADC Considerations

ADC-Ch[0:5] can be connected internally to the successive-approximation 12-bit ADC via a multiplexed input. AD-Ch0 and AD-Ch[6:7] can be configurated as external ADCs , AD-Ch8 is connected to the 1.200 valtage reference source inside the chip. AD-Ch9 is connected to internal temperature sensor.

6.5 User Indicators

The CV90331 supports a variety of options for notifying end-users of the charging status by configuring the GPIO port:

- A piezo-electric buzzer that is supported using GPIO and built-in Timer, which buzzes when the power transfer link is established
- LED visual indicators connected to the LED to notify users of various events
- Defined other status indicators by end-users.

6.6 Over-Voltage and Over-Current Protection

The CV90331 integrates over-voltage protection (OVP) and over-current protection (OCP) shutdown protection

including programmable thresholds. These thresholds are designed to protect the full-bridge and wireless receiver units from exposure to voltages and/or currents that could potentially cause damage or unexpected behavior from the system. For WPC A11 +5 VIN applications, the default OVP level is 6.5V, and this is only monitored during initial power startup. The default OCP level is 2.0A, and this is continuously monitored. The voltage is detected at the VIN pin, and the current is sensed across the R_{SENSE} resistor. If the OCP threshold is exceeded during operation, the CV90331 will cease power transmission and will only resume normal operation after the receiver is removed and replaced on the charging pad or the Tx power is cycled. If an OVP event occurs during startup, the power must be cycled and remain below the OVP threshold during startup for normal operation to occur.

6.7 Thermal Protection

The CV90331 integrates thermal overload shutdown circuitry to prevent damage resulting from excessive thermal stress that could be encountered under fault conditions. This circuitry will shut down or reset the device if the die temperature exceeds the thermal shutdown specification.

To allow the maximum possible load current and to prevent thermal overload, it is important to ensure that the heat generated by the CV90331 solution is dissipated into the PCB. All the available pins must be soldered to the PCB. GND pins (especially the E-PAD) and the external bridge FETs should be soldered to the PCB ground or power planes to improve thermal performance with multiple vias connected to all layers of the PCB. For the QFN package, the exposed paddle (Thermal Pad) must be soldered to the PCB with multiple vias evenly distributed under the package and exiting the bottom side of the PCB. This improves heat flow away from the package and minimizes package thermal gradients.

7. Theory of Operation

The CV90331 is a highly-integrated wireless power transmitter IC solution for mobile devices. It can transfer up to 15W of power in High-Speed- Charger Mode, such as QC2.0/QC3.0/PD2.0/PD3.0 mode or 5W (typical) in WPC mode from a wireless transmitter to an Rx receiver load (e.g., a battery charger) using near-field magnetic induction.

The CV90331 supports Tx configurations such as described in the WPC* v1.2.4 BPP & EPP power profile Tx specification. The CV90331 also embedded Type_C PD and QC2.0/QC3.0 Phy interface and Link engine .

8. Description of the Wireless Power Charging System

A wireless power charging system has a base station with one or more transmitters that make power available DC-to-AC inverter(s) and transmit the power over a strongly-coupled inductor pair to a receiver in a mobile device. A WPC* transmitter could be a *free-positioning* or *magnetically-guided* type. A *free-positioning* type of transmitter has a coil that gives limited spatial freedom to the end-user to align the receiver to the transmitter.

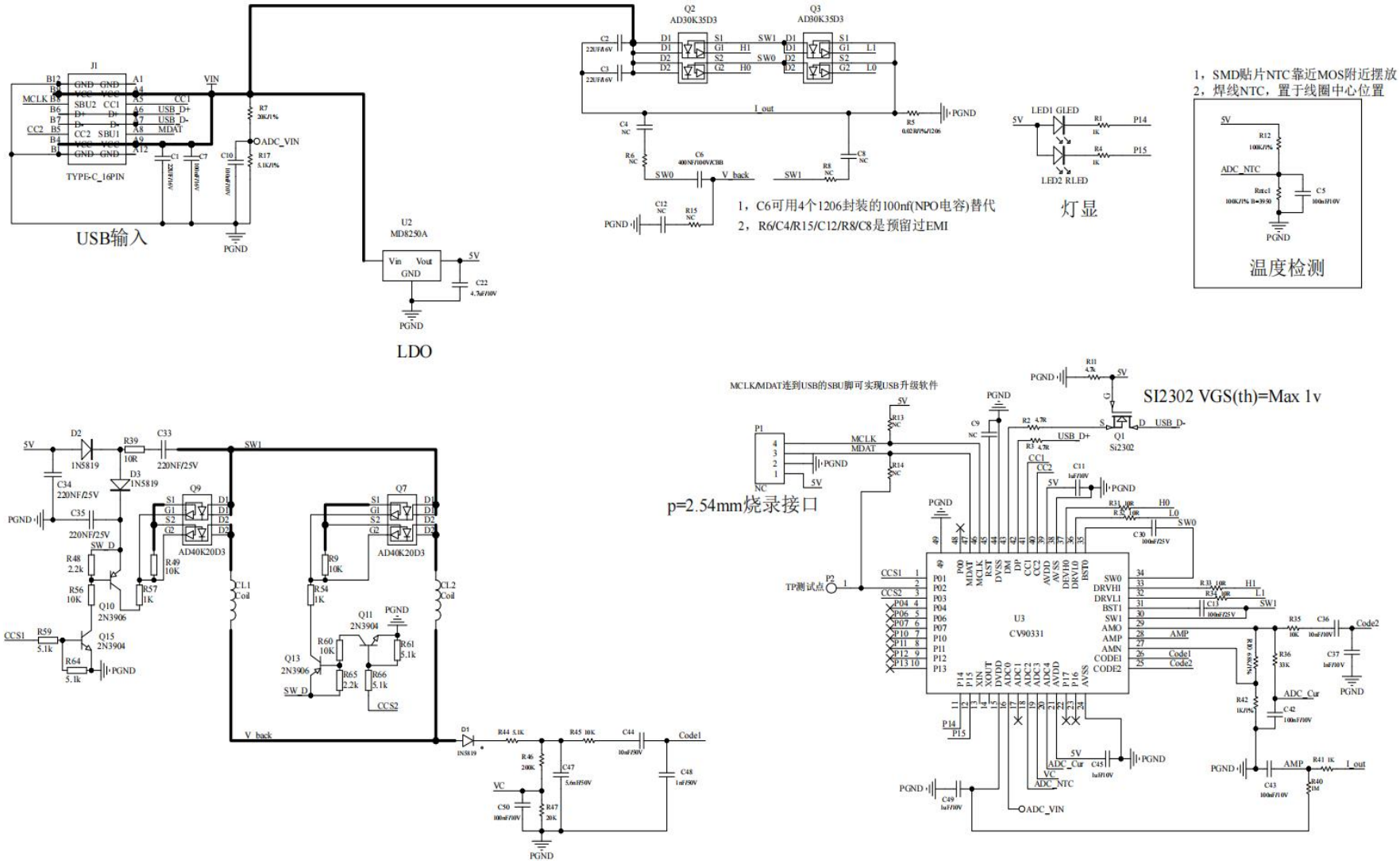
The amount of power transferred to the mobile device is controlled by the receiver. The receiver sends communication packets to the transmitter to increase power, decrease power, or maintain the power level. The communication is purely digital, and communication 1's and 0's ride on top of the power link that exists between the two coils.

A feature of wireless charging system is the fact that when they are not charging a mobile device, the transmitter is in a very-low-power sleep mode. The transmitter remains in this low-power mode and periodically pings until the transmitter detects the presence of a receiver; only after a valid receiver is detected does the transmitter enter the negotiation phase of operation and commence with power transfer.

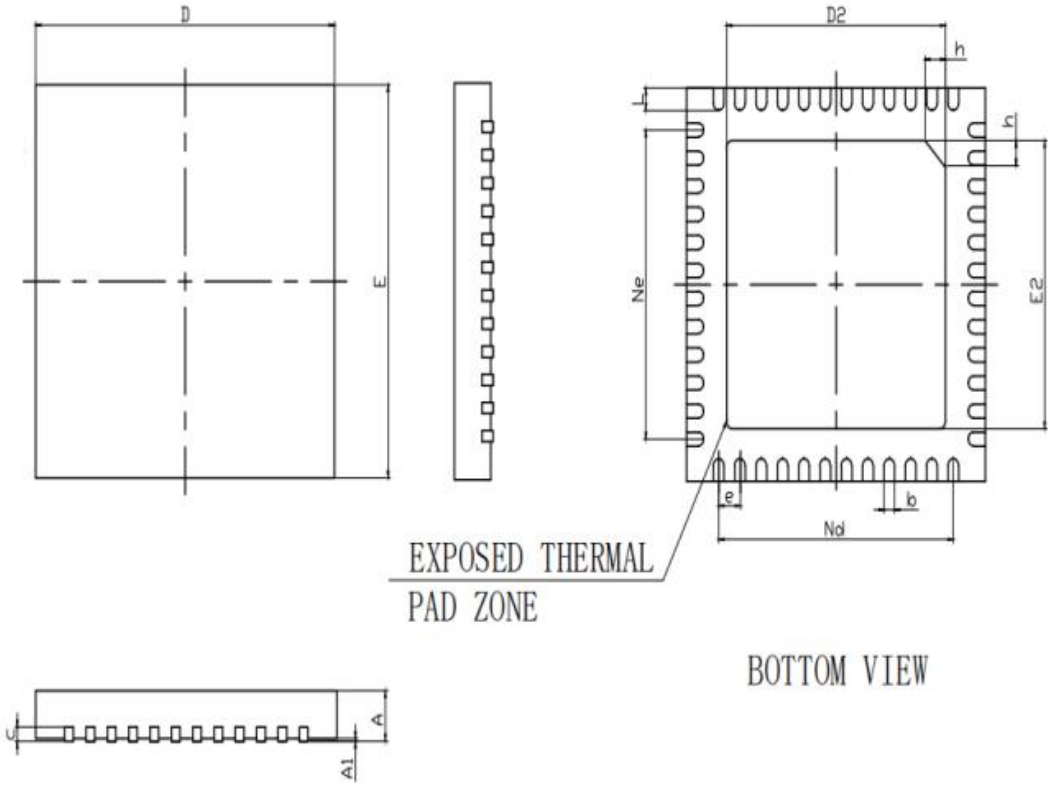
9. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Shipping Packaging	Minimum packing quantity
CV90331	QFN48 (6.00 * 6.00 * 0.75 mm)	MSL3	Reel	3000 PCS

10. Application Schematics



11. Package Drawings



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.20	0.30
D	5.90	6.00	6.10
D2	4.3REF		
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.3REF		
L	0.35	0.40	0.45
h	0.35REF		

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