

1. Description

CV6056D is a System-on-Chip (SoC) that integrates a USB-C port, battery charge/discharge controller, and wireless charging control circuit. It enables a single-chip solution for single USB-C port, single cell battery magnetic power bank products, significantly saving system cost and board space. Both the battery charge/discharge and wireless charging control circuits integrate pre-drivers capable of directly driving MOSFETs. This structure ensures high system efficiency while allowing flexible layout for optimal PCBA thermal dissipation. The USB-C port supports various input/output fast charging protocols such as PPS/PD/SCP/FCP/QC/AFC/BC1.2. It features a built-in boost synchronous buck-boost controller, managing charging and discharging for a single-cell lithium battery. It also integrates wireless charging control circuits and pre-drivers, built-in Q-factor detection, communication decoding circuits, FOD detection, and supports Qi protocols including BPP 5W, Apple Magnetic 7.5W, EPP 15W, Qi2.0(MPP 15W), Qi2.2(MPP 25W), etc.

CV6056D offers high integration, rich I/O interfaces, multiple high-precision ADCs, I2C Master and Slave interfaces, and two built-in SPI interfaces, supporting external SPI Flash and TFT image display functions.

CV6056D features low-power design, wide chip operating voltage range (2.8V ~ 5.5V), and USB-C port bidirectional automatic wake-up detection, ensuring extremely low system quiescent power consumption when implementing a wireless charging power bank system with a single chip. Supports Qi value wake-up for wireless charging.

2. Typical Applications

☆ Qi2.0 & Qi2.2 Magnetic Wireless Charging Power Bank

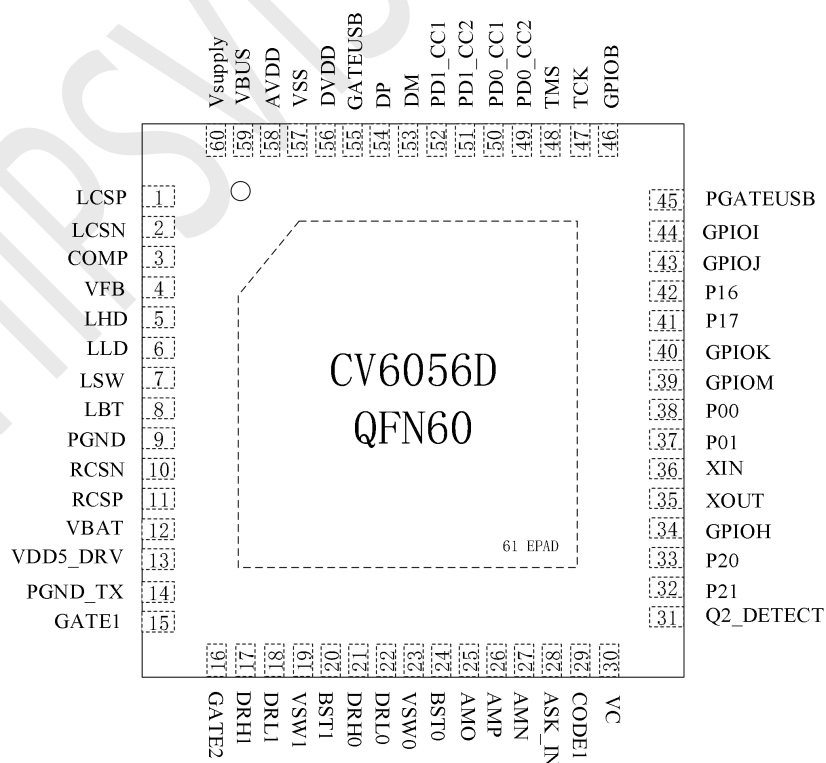
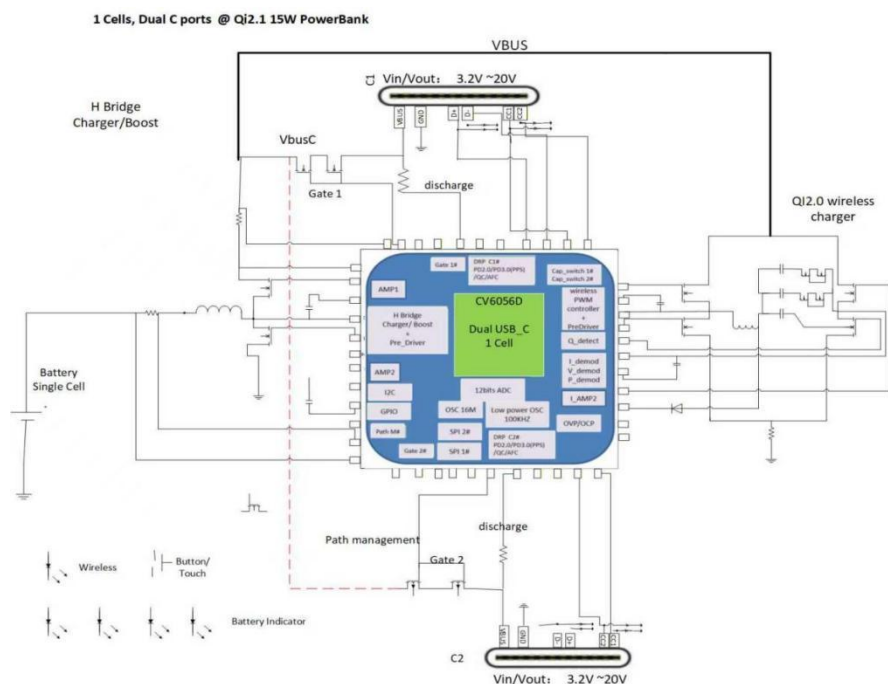
3. Features

- Operating voltage: 2.8V to 5.5V.
- Quiescent current: < 28uA@3.7V.
- Built-in 32-bit processor, supports a maximum operating frequency of 48 MHz.
- 31 channels of 12-bit high-resolution ADC.
- Built-in synchronous buck-boost controller.
- Integrated complete wireless charging circuit.
 - Q-factor detection
 - Current and voltage signal decoding
- High-speed PWM control circuit including dead-time control, PWM adjustment, phase-shift control
- Inverter bridge driver circuit, resonant capacitor switching high-voltage driver circuit
- FOD detection and OCP, OVP, OTP functions
- Built-in master/slave I2C interface, UART for system cascade expansion
- Built-in 2 SPI interfaces, supporting SPI Flash and image display

- Built-in DRP bidirectional full-featured Type-C port controller:
 - Supports PD2.0/PD3.0/PD3.1/PD3.2 PPS
 - Supports CC1/CC2/DP bidirectional low-power wake-up or GPIO wake-up
 - Supports fast charge and fast discharge functions
 - Supports multiple fast charging protocol specifications
 - PD2.0/PD3.0/PD3.1/PD3.2(source/sin) (including Programmable Power Supply PPS)
- Programmable Type-C pull-up resistor/pull-down resistor; built-in VCONN power supply and switch, coordinate E-marker function.
- Supports QC4.0+/QC3.0/QC2.0
 - Supports AFC
 - Supports FCP
 - Supports SCP
 - Supports BC1.2
 - Supports cable impedance compensation
- Charging Specifications
 - Supports single-cell lithium-ion battery charge and discharge management.
 - Input Voltage Range:VBAT to 24V
 - Discharge Specifications
 - Output Voltage:VBAT to 24V
 - Supports single-cell lithium-ion battery charge and discharge management.
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 - Input Voltage Range:VBAT to 24V
 - Discharge Specifications
 - Output Voltage:VBAT to 24V.
 - Output Current:Up to 5A
- Single-Port Output Power Up to 30W.
 - Battery Level Indication
 - Supports percentage battery level display
 - Support Expandable LED Display
 - Supports 188-segment digital tube display.
 - Supports TFT and OLED graphical displays.
 - Wake-up Methods
 - Supports button wake-up
 - Supports USB-C port plug-in wake-up
 - Supports wake-up via touch sensor detection and Q-factor wireless charging detection.
 - Multiple protection mechanisms ensuring safety and reliability.
 - Input Under-Voltage and Over-Voltage Protection
 - Input and Output Over-Current Protection
 - Short-Circuit Protection
 - Battery Overcharge, Overdischarge, and Overcurrent Protection.
 - Chip Over-Temperature and NTC Over-Temperature Protection.
 - The system is resilient, flexible, and reduces BOM cost.

4. Product Information

Orderable Part Number	Package Type	Package Size
CV6056D	QFN60	6.00 * 6.00 * 0.75 mm



6.2 Pin Descriptions

Pin	Name	Description
1	LCSP	DCDC Current Sampling Positive Terminal
2	LCSN	DCDC Current Sampling Negative Terminal
3	COMP	H-Bridge Compensation Pin
4	VFB	H-Bridge Compensation Pin
5	LHD	Buck-Boost High-Side Gate Drive Signal
6	LLD	Buck-Boost Low-Side Gate Drive Signal
7	LSW	Buck-Boost Switching Node (LX Node)
8	LBT	Buckboost High-Side Gate Drive Bias Voltage
9	PGND	Power Ground
10	RCSN	DCDC Current Sense Negative Pin
11	RCSP	DCDC Current Sense Positive Pin
12	VBAT	Battery Voltage Input Pin
13	VDD5_DRV	Internal Driver Power Supply
14	PGND_TX	Power Ground
15	Gate1	Resonant Capacitor Switch MOSFET Gate Drive
16	Gate2	Resonant Capacitor Switch MOSFET Gate Drive
17	DRH1	High-Voltage Half-Bridge Gate Drive Output, Pin 1
18	DRL1	Low-Voltage Half-Bridge Gate Drive Output, Pin 1
19	VSW1	High-Voltage Half-Bridge Switch Node Connection, Pin 1
20	BST1	High-Voltage Half-Bridge Bootstrap Supply, Pin 1
21	DRH0	High-Voltage Half-Bridge Gate Drive Output, Pin 0
22	DRL0	Low-Voltage Half-Bridge Gate Drive Output, Pin 0
23	VSW0	High-Voltage Half-Bridge Switch Node Connection, Pin 0
24	BST0	High-Voltage Half-Bridge Bootstrap Supply, Pin 0
25	AMO	Operational Amplifier Output
26	AMP	Operational Amplifier Non-Inverting Input (+)

27	AMN	Operational Amplifier Inverting Input (-)
28	ASK_IN	Op-Amp Decoding Input
29	CODE1	Current Decoding Input Pin
30	VC	Over-Voltage Protection (OVP) Input
31	Q2_Detect	Q Factor Detection Input 2
32	P21	GPIO P21 Pin
33	P20	GPIO P21 Pin
34	GPIOH	Digital I/O, Analog ADC
35	XOUT	External Crystal Oscillator Input Pin
36	XIN	External Crystal Oscillator Output Pin
37	P01	General-Purpose Digital I/O, Outputs SPI1_MISO
38	P00	General-Purpose Digital I/O, Outputs SPI1_MOSI
39	GPIOM	Digital simulation IO, output SPI1_CS
40	GPIOK/Uart_rx	Digital analog I/O, output SPI1_SCK
41	P17/SDA	General-purpose digital I/O, I2C, clock signal
42	P16/SCL	General-purpose digital I/O, I2C, data signal
43	GPIOJ/INT2	Digital analog I/O, External Interrupt 2, SPI0_MISO
44	GPIOI/INT0	Digital analog I/O, external interrupt 0
45	PGATEUSB	USB Port PMOS Switch Control with Integrated Boost Driver
46	GPIOB/INT1	Digital analog I/O, External Interrupt 1
47	TCK	Simulation/programming interface clock pin
48	TMS	Simulation/Programming Interface Data Pin
49	PD0_CC2	Type-C PD0_CC2 detection pin

50	PD0_CC1	Type-C PD0_CC1 detection pin
51	PD1_CC2	Type-C PD1_CC2 detection pin
52	PD1_CC1	Type-C PD1_CC1 detection pin
53	DM	Connect the USB port DM
54	DP	Connect the USB port DP
55	Gateusb	USB port NMOS switch control, built-in boost driver
56	DVDD	Digital section power supply pin: 1.8V
57	VSS	Power Ground
58	AVDD	5V Power Supply Pin
59	VBUS	VBUS Voltage Sense Pin
60	Vsupply	Output Voltage Sense Pin
61	EPAD	Ground

7. Feature Description

7.1 CPU and Memory

Built-in 32-bit high-performance RISC architecture MCU with 48KB MTP program memory and 7KB SRAM data memory. The device incorporates a 64kHz low-frequency oscillator and a 16MHz high-speed RC main clock oscillator, along with an integrated PLL circuit. The PLL supplies a 48MHz clock to the 32-bit CPU and provides a clock of up to 192MHz for the 16-bit high-speed PWM, ensuring precise frequency variation, pulse-width modulation, and phase shift control in wireless charging applications. A watchdog timer circuit is also integrated.

7.2 USB Type C and PD

7.2.1 USB Type-C Bus Termination and Detection

The source termination resistor (R_p) is implemented by a configurable current source to advertise power capabilities. Attachment/detection is achieved using multiple comparators with different threshold voltages to comply with the Type-C specification. The chip integrates a configurable pull-down resistor (R_d).

When the device operates as a sink, the pull-up resistor (R_p) can be disabled and the pull-down resistor (R_d) enabled. The pull-down resistor is enabled by default upon power-up.

When configured as a source, the Type-C interface enables the pull-up resistor (R_p) and sets the corresponding current level to advertise its power capability.

In Dual-Role Power (DRP) mode, the port alternates between pull-up and pull-down configurations, monitoring the CC1/CC2 pins to determine the sink or source role. Once in low-power mode, the Type-C interface automatically performs attachment detection and wakes up the MCU.

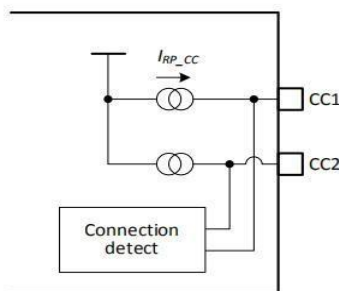


Figure 7.2.1

7.2.2 VCONN

The VCONN supply is switched through an internal MOSFET to deliver power from VDD to the E-Marker cable, with a maximum output of 100 mW. The VCONN switch is controlled by the on-chip MCU and can be turned off after the E-Marker cable is detected to reduce power consumption.

7.2.3 USB BC1.2 、 QC3.0、 QC4.0

The chip is compliant with the USB Battery Charging Specification Revision 1.2 and supports the High Voltage Dedicated Charging Port (HVDCP) QC3.0 protocol. HVDCP utilizes signaling compatible with USB BC1.2 on the D+ and D- lines to negotiate voltage requests on VBUS. QC3.0 is backward compatible with Quick Charge 1.0 and 2.0. Quick Charge 3.0 offers finer voltage increments from 3.6V to 20V in 200mV steps.

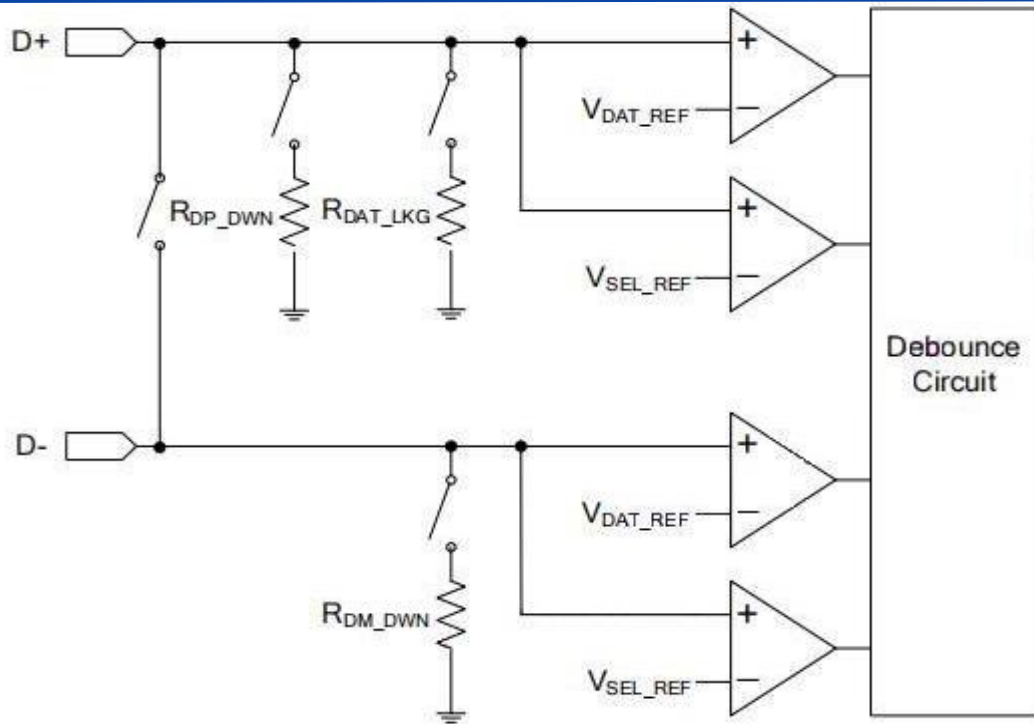


Figure 7.2.3 Internal Circuit Diagram of USB Interface D+ and D- Lines

7.3 boost synchronous charge and discharge

7.3.1 Functional Description of the Charge/Discharge Circuit

The CV6056D integrates a hardware battery charge/discharge controller and MOSFET drivers. It supports peak current detection and features a hardware triangle-wave generator, with an operating frequency configurable from 200kHz to 800kHz. The device incorporates input voltage feedforward and comprehensive protection mechanisms, including Undervoltage Lockout (UVLO), Overvoltage Protection (OVP), Overcurrent Protection (OCP), Short-Circuit Protection (SCP) with alarm, and Overtemperature Protection (OTP). It supports a complete charging cycle management: Trickle Charge, Constant Current (CC) Charge, and Constant Voltage (CV) Charge. The battery termination voltage is software-configurable, supporting charging for various battery types such as 4.2V, 4.35V, 4.4V, and 4.5V batteries. Additionally, it supports a high-efficiency boost discharge mode with an output voltage of up to 24V.

7.4 Buck-Boost DC-DC Converter

7.4.1 Buck-Boost DC-DC Converter typically includes the following configurations:

- Configurable Buck-Boost and Charge/Discharge Operating Modes
- The output voltage is adjustable from VBAT to 24V with a resolution of 20mV.
- High-side current sensing module, to provide constant current and short-circuit current protection.
- Output Overvoltage Protection (OVP)
- Supports an operating frequency range from 200kHz to 800kHz, configurable via software or external resistor.
- Configurable dead time for the driver module to optimize efficiency; configurable maximum and minimum voltage of the DC-DC control triangle wave to adjust the output range.

7.5 Wireless Charging

7.5.1 H-Bridge PWM Control

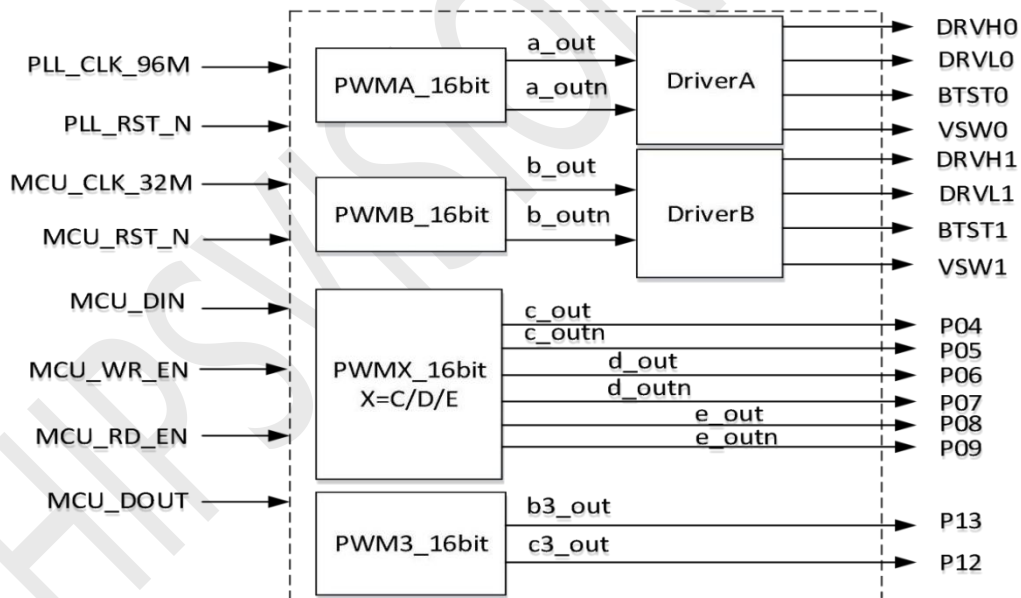


Figure 7.5.1 Full-Bridge PWM Control Diagram

The PWM module operates at a frequency of 156 MHz and integrates five PWM output channels, labeled A through E. Channels A and B form a complementary pair (i_OUT and i_OUTN), as do C and D, while channel E is a single-ended output. Channels A and B each have a dedicated internal driver (Driver A and Driver B, respectively).

Feature Description:

- For each output channel (A/B, C/D, and E), the PWM module provides a 16-bit up-counting auto-reload counter, 16-bit programmable registers for period and duty cycle, and an 8-bit dead-time register.
- Allows the timer registers to be updated after a specified number of counter cycles and repeats the counting process.
- The PWM outputs can be configured to form three independent full-bridge circuits through the pairs A/B, C/D, and A/C. Each bridge operates independently yet remains synchronized with the others, supporting phase shifting, pulse-width modulation, and dead-time adjustment. (Note: The A/C pair can also be configured as a full-bridge.)
 - When configured as a full-bridge pair, channels A and B share the same period and duty-cycle settings while utilizing independent dead-time registers. Channel B's output is phase-shifted with reference to Channel A.
 - When configured as an A/C full-bridge pair, Channels A and C share the period and duty cycle settings (based on Channel A's registers) but utilize independent dead-time configurations. The output of Channel C is phase-shifted relative to Channel A. In this mode, Channel C multiplexes the hardware resources normally assigned to Channel B, allowing Channel D to remain operational independently.
 - When configured as a full-bridge pair, Channels C and D share the period and duty cycle settings (based on Channel C's registers) while utilizing independent dead-time configurations. The output of Channel D is phase-shifted relative to Channel C.
- Channels A, B, and C can be configured to provide four complementary PWM outputs.
 - Share the A_COUNT counter and period register from Channel A.
 - Duty cycle and dead time are configured independently for each channel.
 - The hardware resources of Channel C are multiplexed to Channel D.

- Brake Input with hardware and software brake support.
- Each output pair (i_OUT/i_OUTN) has its own independent output enable control.
- Supports real-time updates to period, duty cycle, dead time, and 360-degree phase shift registers, ensuring the integrity of the PWM cycle.

PWM3_16BIT consists of two independent 16-bit PWM output channels: B3_OUT and C3_OUT.

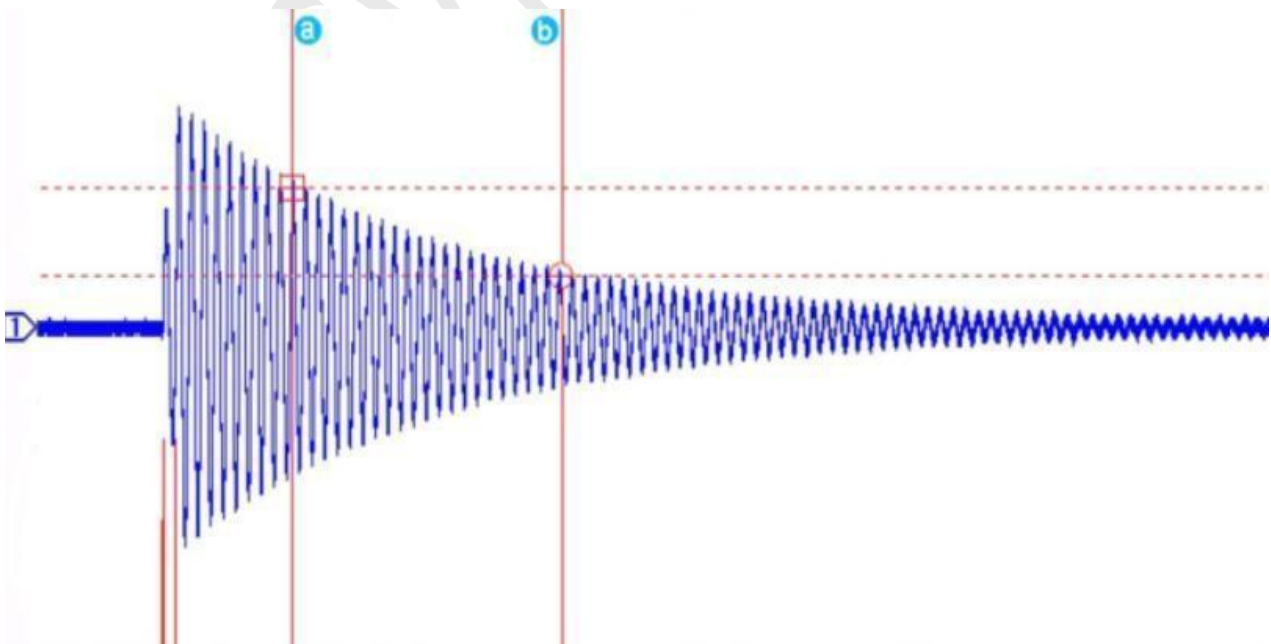
PWM3_16BIT includes a 16-bit auto-reload counter named A_COUNT.

Feature Description:

- Basic Timing.
- Supports simultaneous drive of two independent PWM output channels.

7.6 Q-factor Description

Switch on the high side transistor of the half bridge. Let the LC tank circuit to charge up to a specific energy level before turning on the low side transistor of the half bridge. The LC circuit will then resonate at a high frequency which amplitude decays exponentially.



7.7 Analog ping

The CV6056D sends a short pulse to the LC tank to initiate oscillation. When an RX (receiver) is present, the oscillation amplitude changes, enabling RX detection. This Analog Ping function significantly reduces the average standby power consumption of the TX (transmitter).

7.8 Hardware Over-voltage Protection

CV6056D incorporates a hardware over-voltage protection (OVP) circuit. This enables the chip to implement a fast-triggering protection mechanism, preventing excessive resonant voltage on the coil due to abnormal conditions (such as the presence of a foreign object) from subjecting transmitter system components and the receiving device to high-voltage stress. CV6056 features a triple-stage over-voltage protection mechanism. First Stage: Software Protection, When the VC voltage reaches or approaches a software-preset protection threshold, the software stops increasing the transmitted energy. When the divided voltage from VC (via resistors R1/R2) exceeds the voltage at the comparator's inverting input (3.3V), the hardware protection mechanism is triggered. The OVP signal generates a "Half Bridge Lock" signal, which locks the full-bridge operating mode into a half-bridge mode (Q3 is turned off and Q4 remains constantly on). In this mode, the transmission energy is halved, and an OVP interrupt is generated. If communication between the transmitter (TX) and receiver (RX) remains normal and the VC voltage does not continue to rise, the software can decide whether to resume normal charging. If the VC voltage continues to rise even in half-bridge mode, the system triggers the third protection stage: turning off Q1 and Q3 while keeping Q2 and Q4 MOSFET constantly on, causing the system to enter a discharge state.

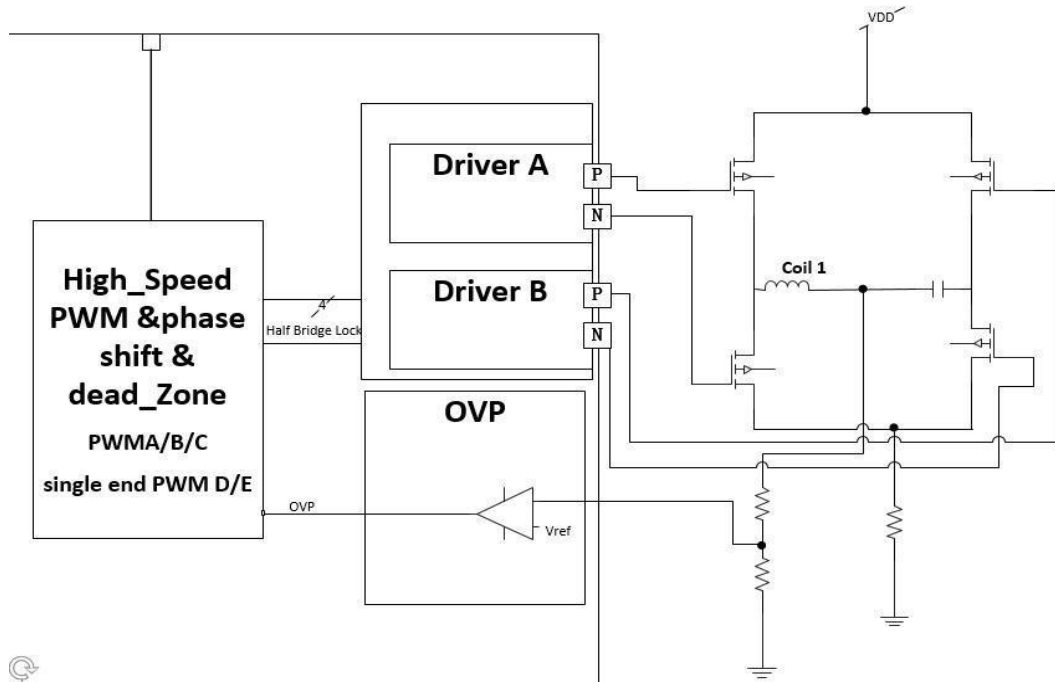


Figure 7.8.1 Hardware Protection circuit Block Diagram

7.9 Foreign Object Detection

The CV6056D utilizes a dual-method approach (Q-factor detection and power loss detection) for Foreign Object Detection (FOD), enabling accurate, rapid judgment and protection:

Q-factor Detection: If the Q-factor detected by the transmitter (TX) is lower than the preset threshold, an FOD alarm is triggered immediately.

Power Loss Detection: The CV6056D integrates a high-precision ADC. If the difference between the TX transmitted power and the RX received power exceeds a preset threshold, the system makes an accurate determination and triggers FOD protection.

7.10 Protection Circuit

7.10.1 OVP and UVP

As shown in Figure 7.10.1, the VCC voltage is compared against a reference voltage generated by the DAC to produce over-voltage (OV) and under-voltage (UV) signals. Simultaneously, the MCU is interrupted, and the control signal (GATE) for the external load switch is removed, turning off the load switch.

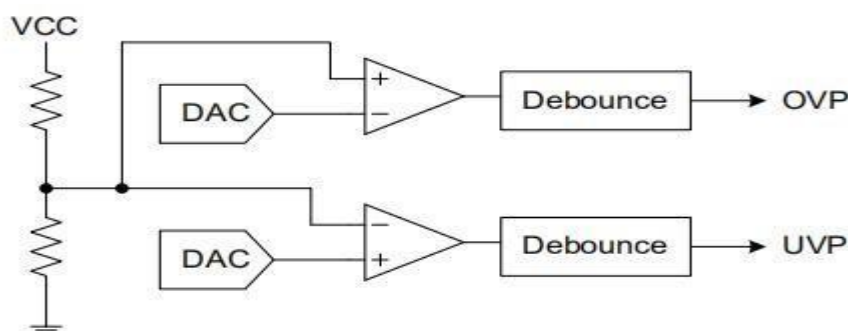


Figure 7.10.1

7.10.2 Over-current Protection

The load current signal is amplified by the current sense amplifier and then digitized by the ADC. Both the over-current trigger threshold and the shaking time are configurable via firmware.

7.10.3 Over-Temperature Protection

The external over-temperature protection for the chip is implemented using a constant current source and a voltage comparator. The current source outputs to an external pin, generating a voltage drop across an NTC thermistor. When this voltage falls below the internally set reference voltage (V_{OTP}), the comparator output triggers an alarm: the GATE signal is disabled and an interrupt is sent to the MCU. The voltage at this pin can also be measured by the ADC.

Select an NTC thermistor with a B-value of 4100K and a nominal resistance of either 200 k Ω or 100 k Ω for the over-temperature protection circuit. The protection trigger point is configurable to 95°C, 105°C, 115°C, or 125°C.

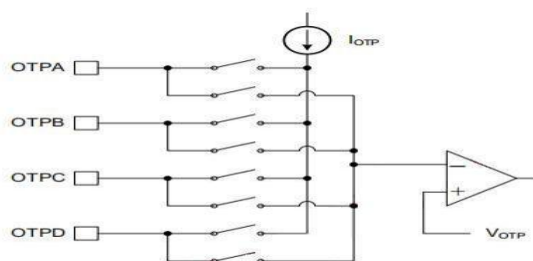


Figure 7.10.3 Schematic Diagram of External Temperature Sensing Component

7.11 On-Chip Temperature Sensing

The chip integrates an on-die temperature sensing circuit. The temperature data read by the MCU is then evaluated to determine whether to trigger over-temperature protection (OTP), depending on the specific application requirements.

7.12 ADC Analog-to-Digital Converter

The on-chip analog-to-digital converter (ADC) features 12-bit resolution and supports more than 20 multiplexed input channels. Specifically, pins P16, P17, GPIO ports C through F, GPIO ports H through K, as well as the ISP and ISN pins, can all be configured as multiplexed ADC inputs via MCU programming.

7.13 Drive signal for the external load switch

An external NMOS power transistor serves as a switch between VCC and VBUS (refer to Section 13, "Typical Application Schematic"). For the switch to turn on, its gate voltage must be higher than the VCC voltage. The internal charge pump generates a sufficiently high gate voltage to turn on the switch when required.

7.14 GPIO

All GPIO pins can be configured as either inputs or outputs.

7.15 Watchdog Timer

The watchdog timer is used to detect CPU malfunctions, such as software lock-ups caused by noise, voltage interference, or power failure. When its internal counter overflows, it generates a reset signal to reset the CPU.

7.16 Reset Function

The chip provides the following reset signals:

- Power-On Reset (POR).
- 1.8V Regulator Output Under-voltage Reset

- VCC Power Supply Under-voltage Protection (UVLO).
- VDD Under-voltage Reset.
- Watchdog Timer Reset.
- Program Counter (PC) Overflow Reset.

8. Electrical Characteristics

8.1 Absolute Maximum Ratings (at an ambient temperature of 25°C)

Parameter	Symbol	Minimum	Maximum	Units
Voltage range	BST0, BST1, DRH0, DRH1 GATEUSB, GATE1, GATE2 LHD, LBT, VBAT,VBUS RCSN,RCSP,Vsupply PGATEUSB,LCSP,LCSN	-0.3	30	V
	VSW0,VSW1,LSW	-0.3	24	V
	PD0_CC1,PD0_CC2 PD1_CC1,PD1_CC2	-0.3	20	V
	DM, DP	-0.3	12	V
	DVDD,XIN,XOUT	-0.3	2	V
	AVSS,PGND,PGND_TX	-0.3	0.3	V
	Other Pin	-0.3	6	V
Junction temperature	T_J		150	°C
Storage temperature	T_{stg}	-40	150	°C
Thermal resistance (junction temperature to environment)	θ_{JA}	30		°C/W
Human Body Model	ESD	-2000	2000	V

8.2 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply Voltage	VIN	2.8		28	V
I/O voltage	PD0_CC1,PD0_CC2 PD1_CC1, PD1_CC2	0	5	5.5	V
Standby power consumption	$I_{standby}$			28	uA
Operating temperature	T_A	-40		85	°C

8.3 Power Characteristics (Operating temperature -20℃ to +105℃)

8.3.1 Power (Vcc, Vdd)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
VCC supply current (normal operation)	ICC_OPR1	VCC ≥ 4.5V, no load on outputs, MCU operating at 10MHz		7		mA
VCC supply current (normal operation)	ICC_OPR2	VCC < 4.5V, no load on outputs, MCU operating at 10MHz		4		mA
Standby current, MCU halted	ICC_STDBY	CC1 or CC2 floating				mA
		CC1 or CC2 connected to a 5.1 kΩ pull-down resistor				mA
VCC Undervoltage Protection (UVP)	VUVLO	VCC rising			2.85	V
		VCC falling	2.6			V
Integrated Regulated Output	VDD		4.75	5	5.25	V

8.3.2 Shunt Regulator

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Voltage Tolerance (Figure 8.3.2)	VOUT	VPWR=23V, Ta=25C, 5V Output			±1.5	%
		VPWR=23V, Ta=25C, 3V ~ 21V Output			±2.5	%
		VPWR=23V, Ta=-20C - 105C, 3V ~ 21V Output			±3.5	%
PPS Voltage Step	Vpps_step	R _{SENSE} =5mΩ, Av=80		20		mV
PPS Current Limit Step	Ipps_step	R _{SENSE} =5mΩ, Av=80		50		mA
Current Limit Tolerance	ΔIPPS_CL	1A ≤ Current Limit Value ≤ 3A			±150	mA
		Current Limit Value > 3A			±5	%

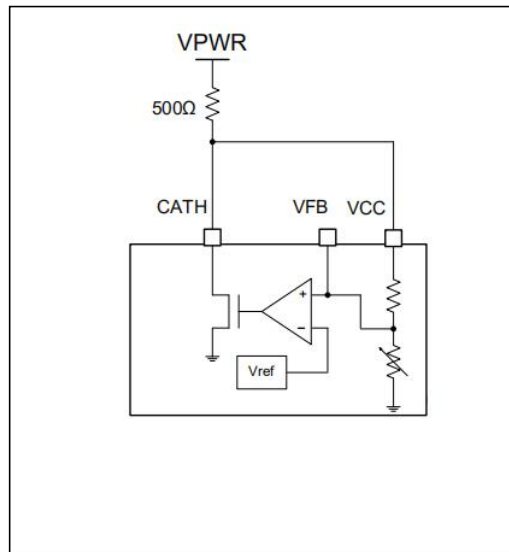


Figure 8.3.2 Test Circuit for the Shunt Regulator

8.3.3 Overvoltage and Undervoltage Protection (OVP, UVLO)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Undervoltage Trigger Point	UVLO				3	V
OVP Step	VOVP_ST EP			0.1		V
OVP Threshold Accuracy	Δ VOVP				± 5	%
UVP Voltage Threshold	VUVP				35	V
UVP Step	VUVP_ST EP			0.1		V
UVP Threshold Accuracy	Δ VUVP				± 5	%

8.3.4 Overcurrent Protection (OCP)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
OCP threshold current	IOCP	$R_s = 5\text{m}\Omega$, $A_v = 80$	0.5		6.4	A
OCP step	Δ IOCP	$R_s = 5\text{m}\Omega$, $A_v = 80$, IOCP=3.6A		0.1		A

8.3.5 ADC

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
ADC Accuracy	NADC			12		bit
ADC INL	INLADC	$T_a = 25^\circ\text{C}$, $V_{in} = 2.5\text{V}$			± 5	LSB
ADC DNL	DNLADC	$T_a = 25^\circ\text{C}$, $V_{in} = 2.5\text{V}$			± 5	LSB
ADC Reference Voltage	VREF_ADC	Option 2.56v/4.3v $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$		2.56		V
				4.3		

8.3.6 CC1, CC2

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
BMC transmitter high-level output	VOH_CC		1.05	1.125	1.2	V
BMC transmitter low-level output	VOL_CC				0.075	V
BMC Receiver High-Level Input	VIH_CC		0.67		1.45	V
BMC Receiver low-Level Input	VIL_CC		-0.25		0.43	V
BMC transmitter output impedance	ZDriver_CC		33		75	Ω
BMC receiver input impedance	ZBMCRX_C C		1			MΩ
Pull-up current source for CC1/CC2	IRP_CC	0.5A@5V		80		μA
		1.5A@5V		180		μA
		3.0A@5V		330		μA
CC1/CC2 detection threshold voltage	VRd_CC	0.5A@5V		1.6		V
		1.5A@5V		1.6		V
		3.0A@5V		2.6		V

8.3.7 VCONN

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
VCONN Voltage	VCONN	VCC = 5V, IVCONN = 0mA		4.85		V
		VCC = 5V, IVCONN = 30mA		3.39		V

8.3.8 USB_D+/D- lines

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Data Signal Detection Voltage	VDAT_REF		0.25	0.35	0.4	V
Selectable Output Voltage	VSEL_REF		1.8			V
D+/D- pull-down resistors	RDWN		14.25		24.8	KΩ
Resistor between D+ and D- (for DCP mode)	RDCP_DA T			30	40	Ω

8.3.9 External Temperature Detection

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Temperature Detection Current Source	IOTP			20.5		μA

8.3.10 On-Chip Temperature Detection

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
On-Chip Temperature Sensor Accuracy	TTS				±10	°C

8.3.11 GPIO

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Low-Level Voltage	VOL_GPIO10m	IOL = 10mA, VDD = 5V VFB, GPIOB, GPIOM-K, P16, P17			0.5	V
GPIO Hi-Z Leakage	IZ_GPIO				10	μA
Input High-level Voltage VTHS=0	VIH	I VFB, GPIOB,, GPIOM-K, P16, P17	0.8*VDD		VDD	V
Input Low-level Voltage VTHS=0	VIL	VFB, GPIOB GPIOM-K, P16, P17	0		0.2*VDD	V
Input High-level Voltage VTHS=1	VIH	VFB, GPIOB, GPIOM-K, P16, P17	0.52*VDD		VDD	V
Input Low-level Voltage VTHS=1	VIL	VFB, GPIOB, GPIOM-K, P16, P17	0		0.13*VDD	V

8.3.12 DC-DC Buck-Boost Converter

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Voltage Level	Vout_sel	Iout = 1mA	3.2		34	V
Maximum OVP Threshold	Ovp_rise	Vout > Set Point, Trip the OVP	112.5		120	%
Minimum OVP Threshold	Ovp_fall	Vout < Set Point, Resume normal operation.	90		100	%

8.4 AC Characteristics (Vcc=20V, Temperature Range: -20°C to +105°C)

8.4.1 Internal Oscillator

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Main Oscillator Frequency	Foscm			16		MHz
Low-Frequency Clock Oscillator	Fosca			64		KHz

8.4.2 USB-PD BMC Transmitter and Receiver

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
BMC Data Rate	f _{BMC}		270	300	330	KHz

BMC Transmitter Rise Time	t_{RISE_BMC}		300			ns
BMC Transmitter Fall Time	t_{FALL_BMC}		300			ns
Time from Last Rising Edge to Drive Termination	t_{HOLD_BMC}		1			μs
Packet-to-Packet Interval	t_{IFG_BMC}		25			μs
Data End to Drive-Off Time	t_{END_EMC}				23	μs
BMC Receiver Bandwidth Limiting Window	t_{RXFTR_BMC}		100			ns
Non-Idle Detection Window	t_{NIDLE_BMC}		12		20	μs
Level transition required to exit the idle state	N_{NIDLE_BMC}		3			
Pulse Width for Logic '1' (BMC Transmitter)	t_{PULSE1_BMC}	Ta = 25°C, Total CC Capacitance = 1010pF, CC Pin Series Resistance = 47Ω		1.4	1.8	μs

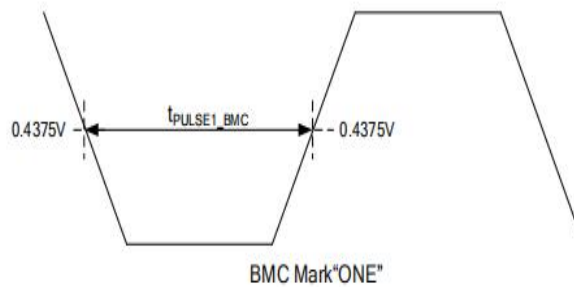


Figure 8.4.2a BMC Timing Diagram

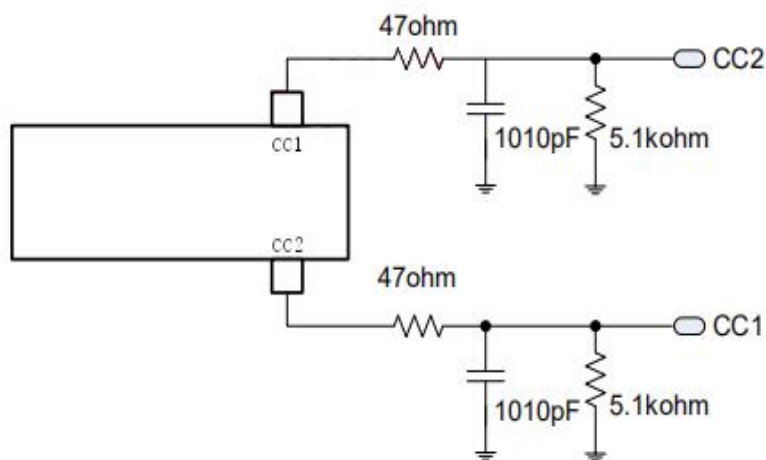


Figure 8.4.2b BMC Transmitter Logic '1' Pulse Width Test Circuit

8.4.3 DC-DC Buck-Boost Converter

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Switching Frequency	fdcdc		190	390	755	KHz
Drive Dead Time	Driver_dt		39		140	ns
Debounce Delay	debounce		100		200	ns

9. Application Schematic

The application schematic for the CV6056D product can be found on the last page.

10. Package Information

Refer to page 23 for package outline drawing.

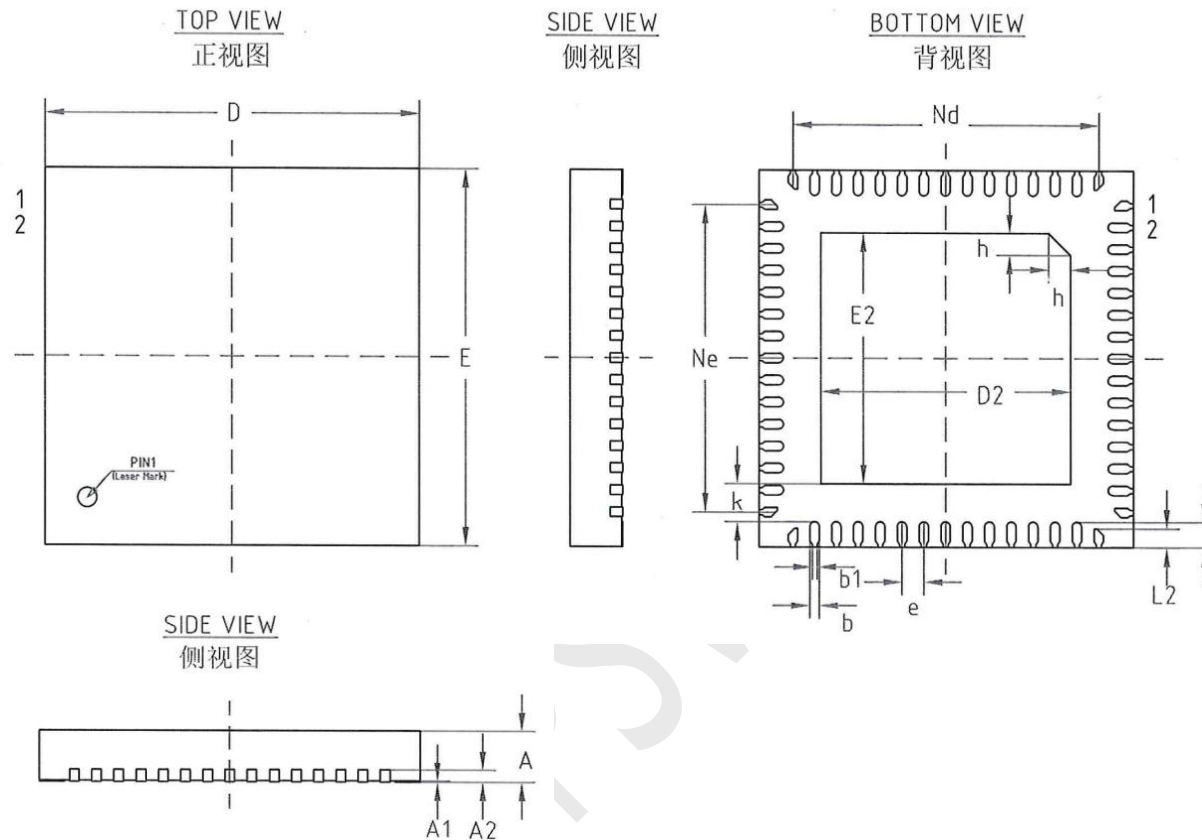
Part Number	Package	MSL	Packaging	MPQ
CV6056D	QFN60 (6.00 * 6.00 * 0.75 mm)	Level 3	Reel	3000 PCS

11. Marking Diagram



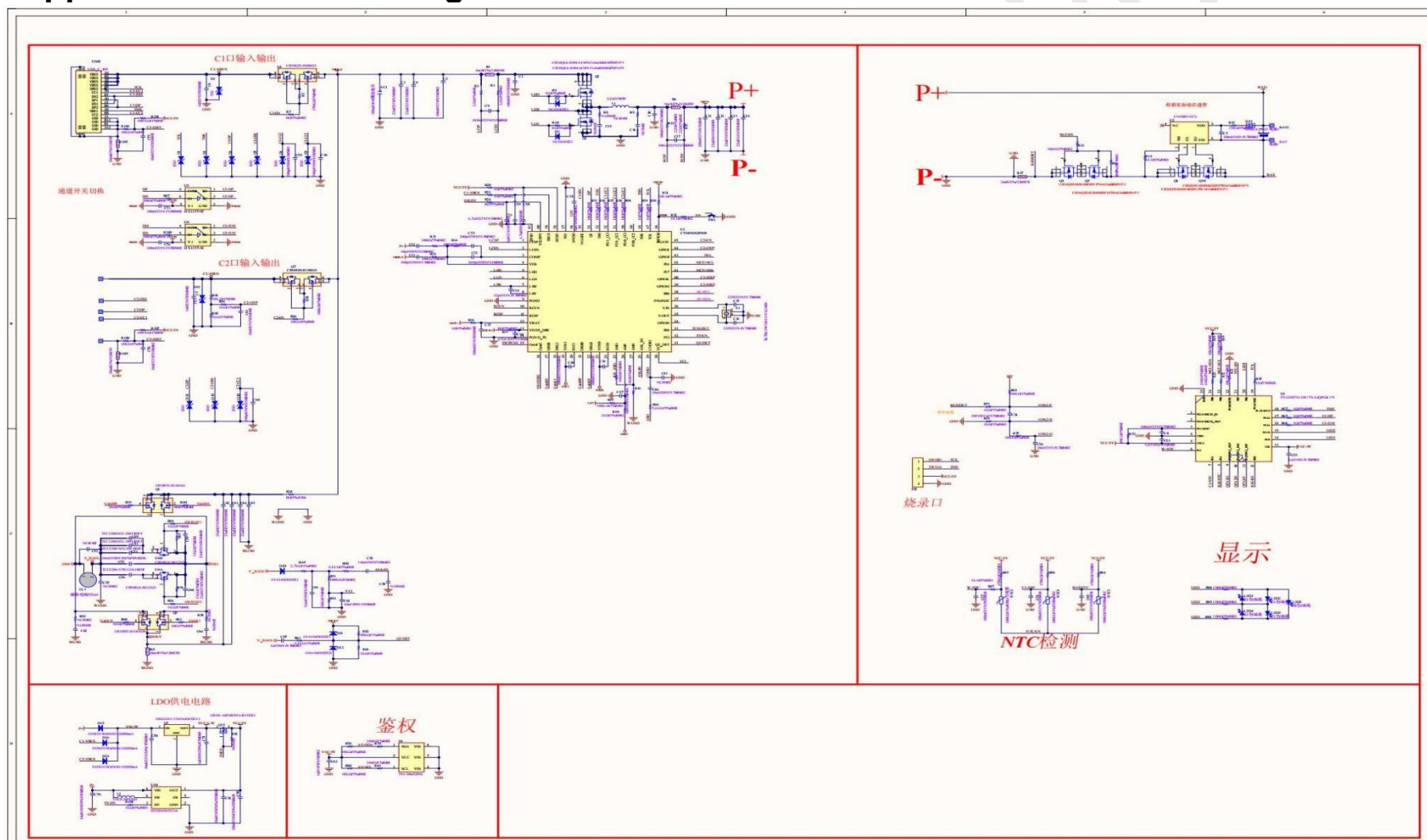
Position	Marking Content	Meaning
Line 1	CVSMicro	Company name
Line 2	CV6056D	The part number
Line 3	XXXXXX	Lot Number

12. Package Outline Drawing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
A2	0.203REF		
b	0.10	0.15	0.20
b1	0.08REF		
D	5.9	6	6.1
E	5.9	6	6.1
D2	3.9	4	4.1
E2	3.9	4	4.1
e	0.35BSC		
K	0.50	0.60	0.70
L	0.30	0.40	0.50
L2	0.30REF		
h	0.30	0.35	0.40
Nd	4.90BSC		
Ne	4.90BSC		

13. Application schematic diagram



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