A Low Quiescent Power Qi2.0 & Qi2.2 Wireless Charging SoC

1 Description

The CV90367C is a System-on-Chip (SoC) that integrates a USB-C port with wireless charging control circuit. It features a built-in high-voltage driver for tank capacitors and is designed with an ultra-low power consumption architecture. This chip is suitable for Qi2.0 & Qi2.2 wireless charging products, making it particularly suitable for wireless charging power banks with Q-factor detection functionality. the USB-C port supports multiple sink fast-charging protocols such as UFCS, PPS, PD, SCP, FCP, QC, AFC, and BC1.2, as well as PD and QC source fast-charging protocols. Built in wireless charging control circuit and pre driver circuits, and built-in Q-factor detection, communication decoding circuit, and Foreign Object Detection (FOD). It supports multiple Qi protocols such as BPP 5W , Apple MagSafe 7.5W, EPP 15W, Qi2.0(MPP 15W), and Qi2.2(MPP 25W),Power transfer up to 80W in proprietary mode.

CV90367C boasts a high level of integration and rich I/O interface functionality. It incorporates multiple channels of high-precision ADC and features both I2C Master and Slave interfaces. The chip also integrates two SPI interfaces, supporting external SPI Flash and TFT image display functions.

CV90367C adopts a low-power design with a wide operating voltage range of 2.8V to 5.5V. It supports wireless charging wake-up via Q-factor detection, ensuring extremely low system quiescent power consumption.

2 Applications

- Magnetic Wireless Charging Power Bank.
- Magnetic Wireless Charging Portable Device.

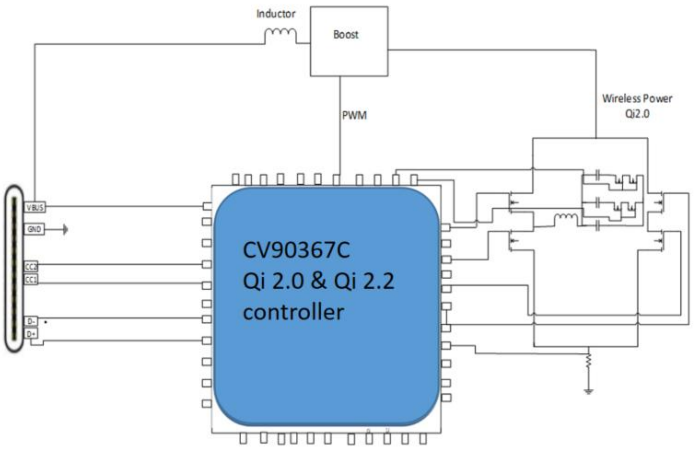
3 Features

- Operating Voltage Range: 2.8V to 5.5V
- Standby current: <28uA @ 3.8V
- Integrated 32-bit processor with CPU operating frequency up to 50 MHz.
- 31-channel 12-bit high-precision ADC
- Built-in complete set of wireless charging circuits
  - Q-factor detection
  - Current and voltage demodulation
  - High-speed PWM controller featuring dead-time control; PWM duty-cycle adjustment; and phase-shift control.
  - FOD detection with OCP, OVP, and OTP protection

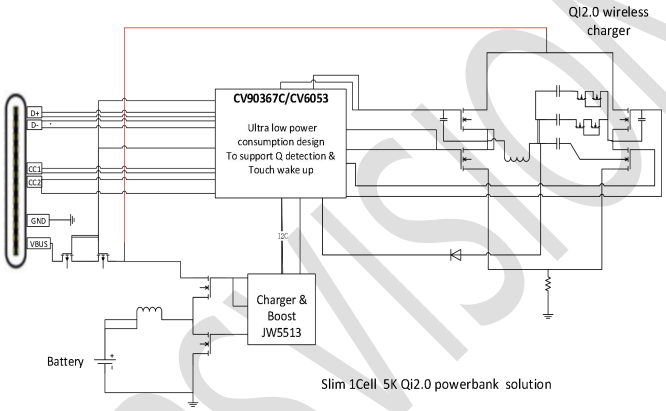
- Integrated master/slave I2C interface and UART for system cascading and expansion.
- Built-in 2 SPI: supports external SPI Flash and display.
- Fully-integrated bidirectional Type-C port controller：
  - Supports with PD2.0, PD3.1, and PPS
  - Supports low-power wake-up via bidirectional CC1/CC2/DP pins or GPIO.
  - Supports fast charging and fast discharging.
- ◆ Supports multiple fast charging protocols.
  - Supports PD2.0/PD3.0/PD3.1 (sink) including Programmable Power Supply (PPS).
  - Features programmable pull-up and pull-down resistors for Type-C configuration. Includes an integrated VCONN power supply and switch to support E-Marker cable detection
  - Supports QC4.0+/QC3.0/QC2.0
  - Supports AFC
  - Support FCP
  - Support SCP
  - BC1.2 compliant
- Wake-up Sources
  - Supports wake-up via touch or Q-factor detection.
- Comprehensive protection mechanisms ensure safety and reliability.
  - Input Under-voltage and Over-voltage Protection
  - Input and Output Over-current Protection
  - Short-Circuit Protection
  - Battery Overcharge, Over-Discharge, and Over-current Protection
  - Internal Die Over-Temperature and External NTC Over-Temperature Protection
- Enhanced system resilience and design flexibility enable BOM cost reduction.
- QFN-56 package, 6 mm x 6 mm body size

1 Qi2.0 & Qi2.2 Wireless Charging System Block Diagram

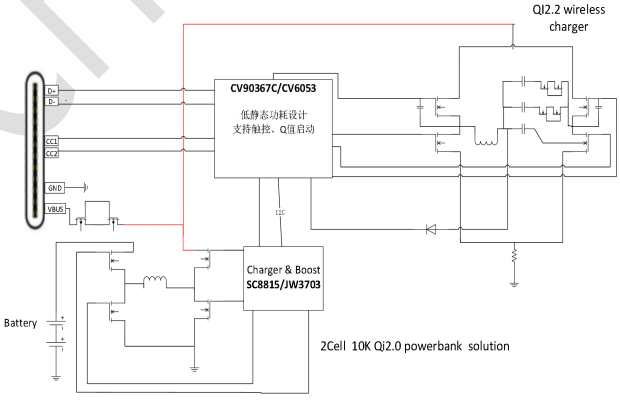
1.1 Qi2.0 & Qi2.2 Magnetic wireless charging application



1.2 Single cell battery magnetic wireless charging mobile power application

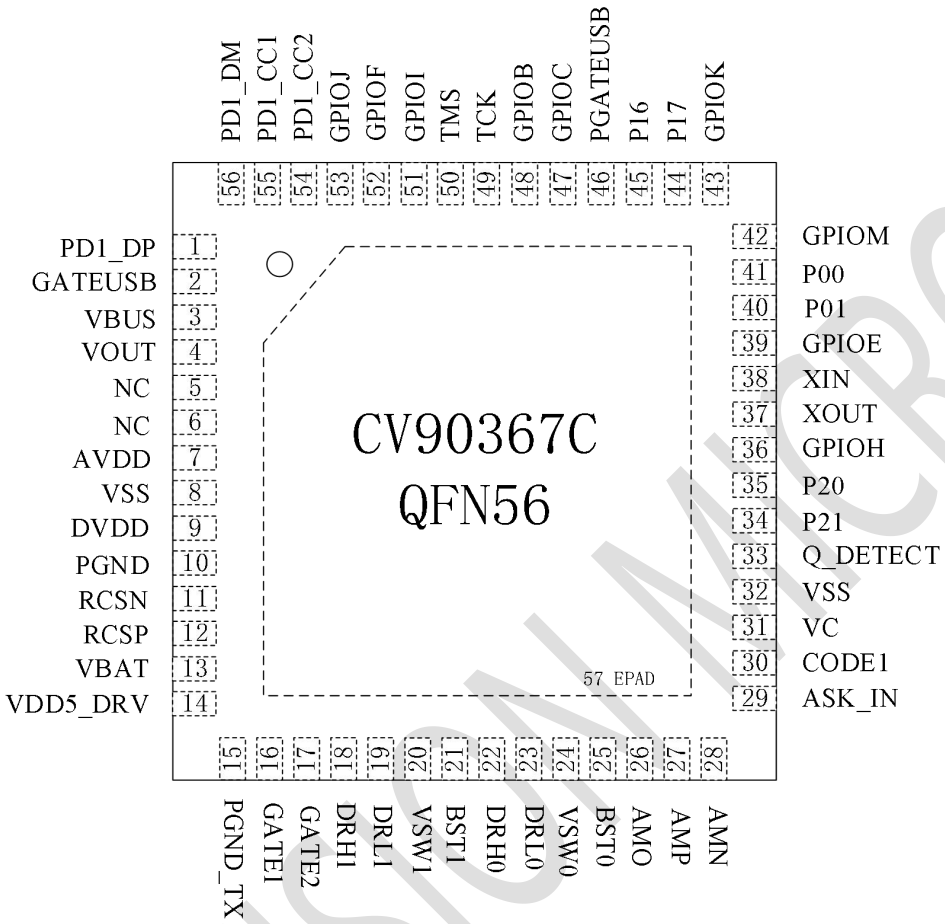


1.3 Multi cell battery magnetic wireless charging mobile power application



2 Pin Definitions and Descriptions

2.1 Pin Assignments



2.2 CV90367C Pin Descriptions

Pin Number	Name	Description
1	PD1_DP	USB D+ interface
2	GATEUSB	Integrated NMOS power switch for USB port control; built-in boost driver.
3	VBUS	VBUS_C Port Positive Voltage Detection
4	VOUT	Output voltage detection; CSN (current sense negative) for current sampling.
5	NC	NC
6	NC	NC
7	AVDD	5V internal LDO
8	VSS	Ground
9	DVDD	1.8V

10	PGND	Power Ground
11	RCSN	VBUS Pin Current Sense Negative
12	RCSP	VBUS Pin Current Sense Positive
13	VBAT	VBAT Power Supply and Cell Monitoring
14	VDD5_DRV	Internal Driver Supply
15	PGND_TX	Power Ground
16	GATE1	Tank Capacitor Switching MOSFET Driver
17	GATE2	Tank Capacitor Switching MOSFET Driver
18	DRH1	MOSET Half-Bridge Driver 1 High-Side output
19	DRL1	MOSET Half-Bridge Driver 1 Low-Side output
20	VSW1	MOSFET Half-Bridge Driver 1 High-side source connection.
21	BST1	MOSFET Half-Bridge Driver 1 High-side bootstrap supply
22	DRH0	MOSET Half-Bridge Driver 0 High-Side output
23	DRL0	MOSET Half-Bridge Driver 0 Low-Side output
24	VSW0	MOSFET Half-Bridge Driver 0 High-side source connection.
25	BST0	MOSFET Half-Bridge Driver 0 High-side bootstrap supply
26	AMO	Op-amp positive output terminal
27	AMP	Op-amp positive input terminal
28	AMN	Op-amp nagtive input terminal
29	ASK_IN	Input pin for phase signal demodulation
30	CODE1	Current Demodulation Signal
31	VC	Over-voltage Protection Input Pin
32	VSS	Ground
33	Q_DETECT	Q-factor Detection Input Pin
34	P21	General-purpose digital I/O pin
35	P20	General-purpose digital I/O pin
36	GPIOH	Digital/Analog I/O

37	XOUT	External crystal output pin
38	XIN	External crystal input pin
39	GPIOE	Digital/Analog I/O ADC Input Channel
40	P01	General-purpose digital I/O pin
41	P00	General-purpose digital I/O pin
42	GPIOM	Digital/Analog I/O ADC Input Channel
43	GPIOK	Digital/Analog I/O ADC Input Channel
44	P17	General-purpose digital I/O pin
45	P16	General-purpose digital I/O pin
46	PGATEUSB/OD	Integrated NMOS power switch for USB port control; built-in boost driver. Open Drain pin
47	GPIOC	Digital/Analog I/O ADC Input Channel Comp2 Pin
48	GPIOB	Digital/Analog I/O INT1 Pin
49	TCK	Emulation port clock pin
50	TMS	External crystal input pin
51	GPIOI	Digital/Analog I/O ADC Input Channel INT0 Pin
52	GPIOF	Digital/Analog I/O ADC Input Channel
53	GPIOJ	Digital/Analog I/O ADC Input Channel
54	PD1_CC2	Type-C CC2 detection pin
55	PD1_CC1	Type-C CC1 detection pin
56	PD1_DM	USB D- interface
57	PGND	Power Ground

3 Functional Description

3.1 CPU and Memory

The chip integrates a 32-bit high-performance RISC MCU, 48 KB of MTP program memory, and 7 KB of SRAM. It contains a 64 kHz low-frequency oscillator and a 16 MHz high-speed RC main oscillator. An on-chip PLL generates a 32 MHz clock for the CPU and a clock up to 156 MHz for the 16-bit high-speed PWM, ensuring precision in frequency variation, PWM, and phase-shift control for wireless charging. A built-in watchdog circuit is included.

3.2 USB Type C and PD

3.2.1 USB Type C Bus Termination and Detection

The source termination resistor (Rp) is implemented by a configurable current source to advertise power capabilities. Attachment/detection is achieved using multiple comparators with different threshold voltages to comply with the Type-C specification.The chip integrates a configurable pull-down resistor (Rd).

When the device operates as a sink, the pull-up resistor (Rp) can be disabled and the pull-down resistor (Rd) enabled. The pull-down resistor is enabled by default upon power-up.

When configured as a source, the Type-C interface enables the pull-up resistor (Rp) and sets the corresponding current level to advertise its power capability.

In Dual-Role Power (DRP) mode, the port alternates between pull-up and pull-down configurations, monitoring the CC1/CC2 pins to determine the sink or source role.

Once in low-power mode, the Type-C interface automatically performs attachment detection and wakes up the MCU.

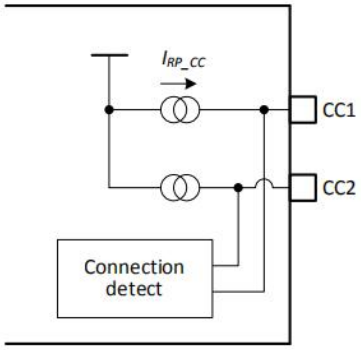


Figure 3.2.1

3.2.2 VCONN

The VCONN supply is switched through an internal MOSFET to deliver power from VDD to the E-Marker cable, with a maximum output of 100 mW. The VCONN switch is controlled by the on-chip MCU and can be turned off after the E-Marker cable is detected to reduce power consumption.

3.2.3 USB BC1.2 、QC3.0、QC4.0

The chip is compliant with the USB Battery Charging Specification Revision 1.2 and supports the High Voltage Dedicated Charging Port (HVDCP) QC3.0 protocol. HVDCP utilizes signaling compatible with USB BC1.2 on the D+ and D- lines to negotiate voltage requests on VBUS. QC3.0 is backward compatible with Quick Charge 1.0 and 2.0. Quick Charge 3.0 offers finer voltage increments from 3.6V to 20V in 200mV steps.

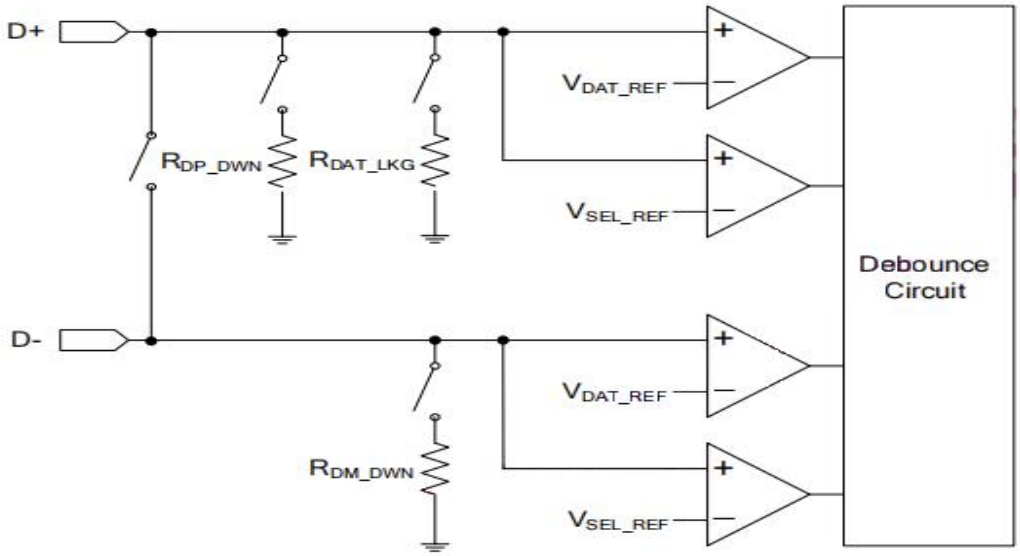


Figure 3.2.3 Internal Circuit Diagram of USB Interface D+ and D- Lines

3.3 Wireless Charging

3.3.1 Full-Bridge PWM Control

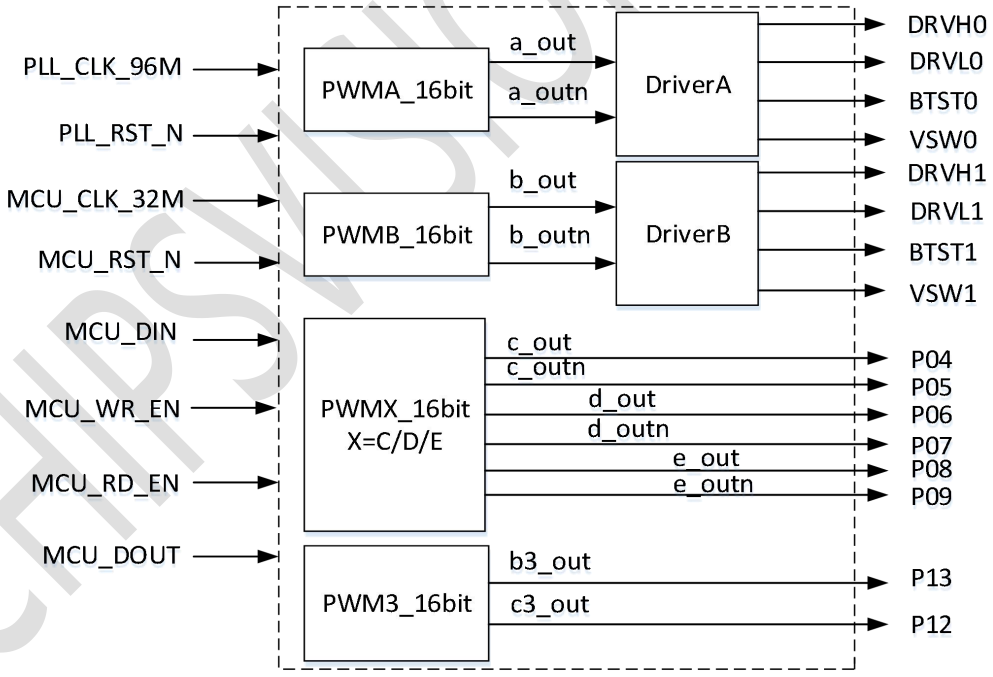


Figure 3.3.1 Full-Bridge PWM Control Diagram

The PWM module operates at a frequency of 156 MHz and integrates five PWM output channels, labeled A through E. Channels A and B form a complementary pair (i_OUT and i_OUTN), as do C and D, while channel E is a single-ended output.

Channels A and B each have a dedicated internal driver (Driver A and Driver B, respectively).

Feature Description：

- For each output channel (A/B, C/D, and E), the PWM module provides a 16-bit up-counting auto-reload counter, 16-bit programmable registers for period and duty cycle, and an 8-bit dead-time register.
- Allows the timer registers to be updated after a specified number of counter cycles and repeats the counting process.
- The PWM outputs can be configured to form three independent full-bridge circuits through the pairs A/B, C/D, and A/C. Each bridge operates independently yet remains synchronized with the others, supporting phase shifting, pulse-width modulation, and dead-time adjustment. (Note: The A/C pair can also be configured as a full-bridge.)

- When configured as a full-bridge pair, channels A and B share the same period and duty-cycle settings while utilizing independent dead-time registers. Channel B's output is phase-shifted with reference to Channel A.
- When configured as an A/C full-bridge pair, Channels A and C share the period and duty cycle settings (based on Channel A's registers) but utilize independent dead-time configurations. The output of Channel C is phase-shifted relative to Channel A. In this mode, Channel C multiplexes the hardware resources normally assigned to Channel B, allowing Channel D to remain operational independently.
- When configured as a full-bridge pair, Channels C and D share the period and duty cycle settings (based on Channel C's registers) while utilizing independent dead-time configurations. The output of Channel D is phase-shifted relative to Channel C.

- Channels A, B, and C can be configured to provide four complementary PWM outputs.

- Share the A_COUNT counter and period register from Channel A.

- Duty cycle and dead time are configured independently for each channel.
- The hardware resources of Channel C are multiplexed to Channel D.

- Brake Input with hardware and software brake support.
- Each output pair (i_OUT/i_OUTN) has its own independent output enable control.
- Supports real-time updates to period, duty cycle, dead time, and 360-degree phase shift registers, ensuring the integrity of the PWM cycle.

PWM3_16BIT consists of two independent 16-bit PWM output channels: B3_OUT and C3_OUT.

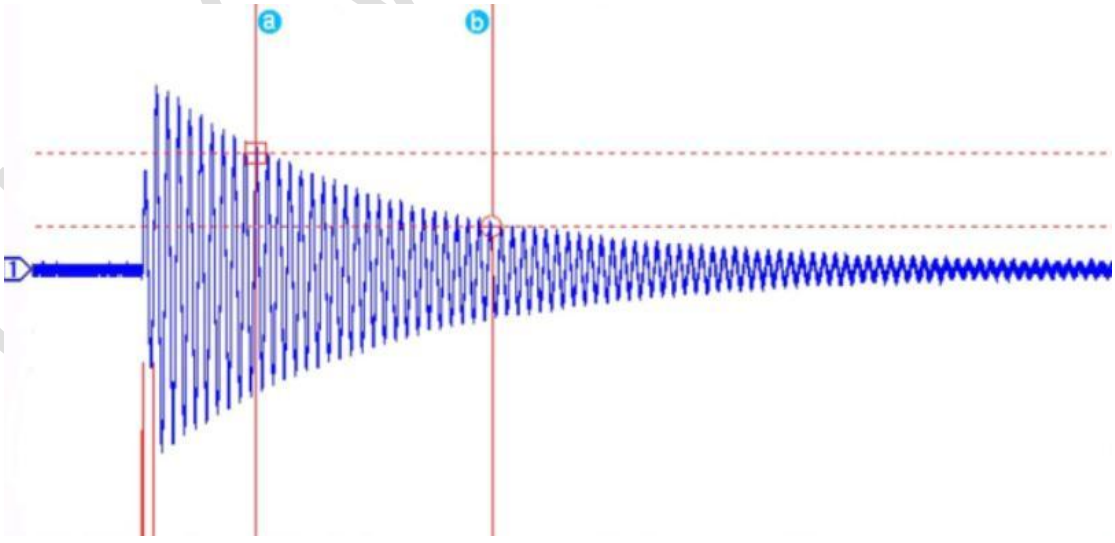
PWM3_16BIT includes a 16-bit auto-reload counter named A_COUNT.

Feature Description：

- Basic Timing.
- Supports simultaneous drive of two independent PWM output channels.

3.4 Q-factor Detection

Switch on the high side transistor of the half bridge. Let the LC tank circuit to charge up to a specific energy level before turning on the low side transistor of the half bridge. The LC circuit will then resonate at a high frequency which amplitude decays exponentially.



3.5 Analog ping

The CV90367C sends a short pulse to the LC tank to initiate oscillation. When an RX (receiver) is present, the oscillation amplitude changes, enabling RX detection. This Analog Ping function significantly reduces the average standby power consumption of the TX (transmitter).

3.6 Hardware Over-voltage Protection

CV90367C incorporates a hardware over-voltage protection (OVP) circuit. This enables the chip to implement a fast-triggering protection mechanism, preventing excessive resonant voltage on the coil due to abnormal conditions (such as the presence of a foreign object) from subjecting transmitter system components and the receiving device to high-voltage stress. CV90367C features a triple-stage over-voltage protection mechanism. First Stage: Software Protection， When the VC voltage reaches or approaches a software-preset protection threshold, the software stops increasing the transmitted energy. When the divided voltage from VC (via resistors R1/R2) exceeds the voltage at the comparator's inverting input (3.3V), the hardware protection mechanism is triggered. The OVP signal generates a "Half Bridge Lock" signal, which locks the full-bridge operating mode into a half-bridge mode (Q3 is turned off and Q4 remains constantly on). In this mode, the transmission energy is halved, and an OVP interrupt is generated. If communication between the transmitter (TX) and receiver (RX) remains normal and the VC voltage does not continue to rise, the software can decide whether to resume normal charging. If the VC voltage continues to rise even in half-bridge mode, the system triggers the third protection stage: turning off Q1 and Q3 while keeping Q2 and Q4 MOSFET constantly on, causing the system to enter a discharge state.

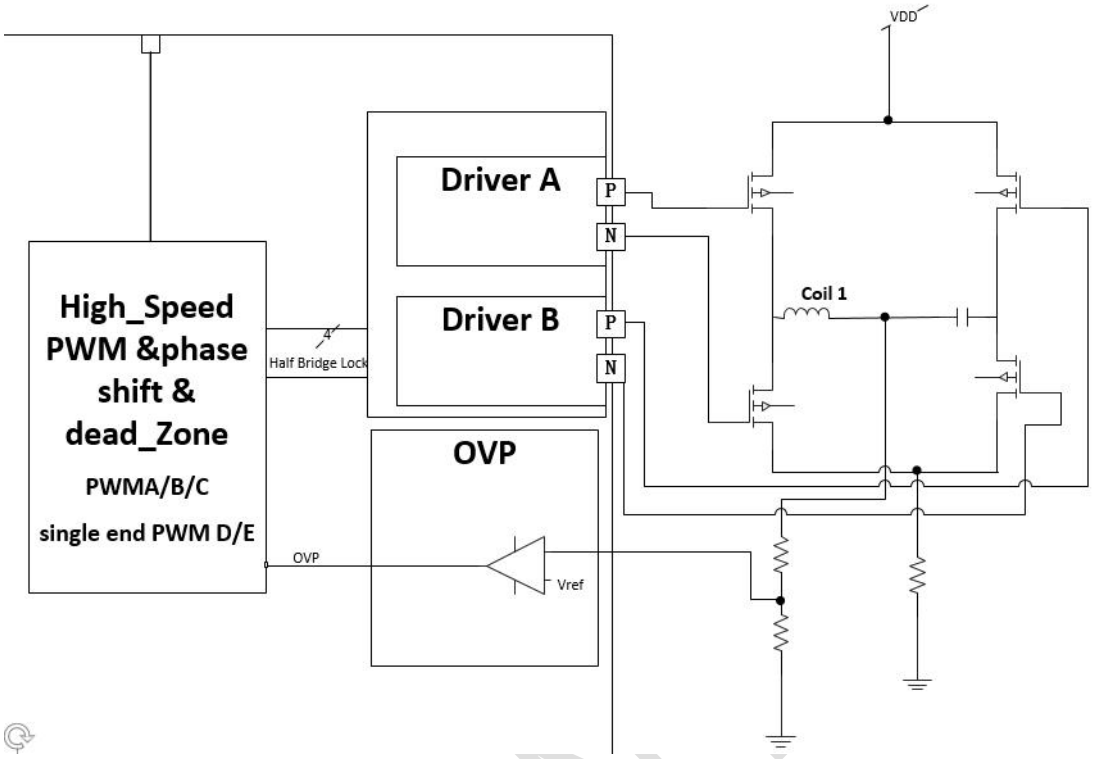


Figure 3.6.1 Hardware Protection circuit Block Diagram

3.7 Foreign Object Detection

The CV90367C utilizes a dual-method approach (Q-factor detection and power loss detection) for Foreign Object Detection (FOD), enabling accurate, rapid judgment and protection:

- Q-factor Detection：If the Q-factor detected by the transmitter (TX) is lower than the preset threshold, an FOD alarm is triggered immediately.
- Power Loss Detection：The CV90367C integrates a high-precision ADC. If the difference between the TX transmitted power and the RX received power exceeds a preset threshold, the system makes an accurate determination and triggers FOD protection.

3.8 Protection Circuit

3.8.1 OVP and UVP

As shown in Figure 3.10.1, the VCC voltage is compared against a reference voltage generated by the DAC to produce over-voltage (OV) and under-voltage (UV) signals. Simultaneously, the MCU is interrupted, and the control signal (GATE) for the external load switch is removed, turning off the load switch.

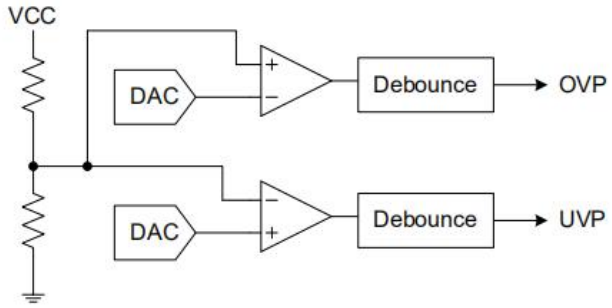


Figure 3.8.1

3.8.2 Over-current Protection

The load current signal is amplified by the current sense amplifier and then digitized by the ADC. Both the over-current trigger threshold and the debounce time are configurable via firmware.

3.8.3 Over-Temperature Protection

The external over-temperature protection for the chip is implemented using a constant current source and a voltage comparator. The current source outputs to an external pin, generating a voltage drop across an NTC thermistor. When this voltage falls below the internally set reference voltage (V_OTP), the comparator output triggers an alarm: the GATE signal is disabled and an interrupt is sent to the MCU. The voltage at this pin can also be measured by the ADC.

Select an NTC thermistor with a B-value of 4100K and a nominal resistance of either 200 kΩ or 100 kΩ for the over-temperature protection circuit. The protection trigger point is configurable to 95°C, 105°C, 115°C, or 125°C.

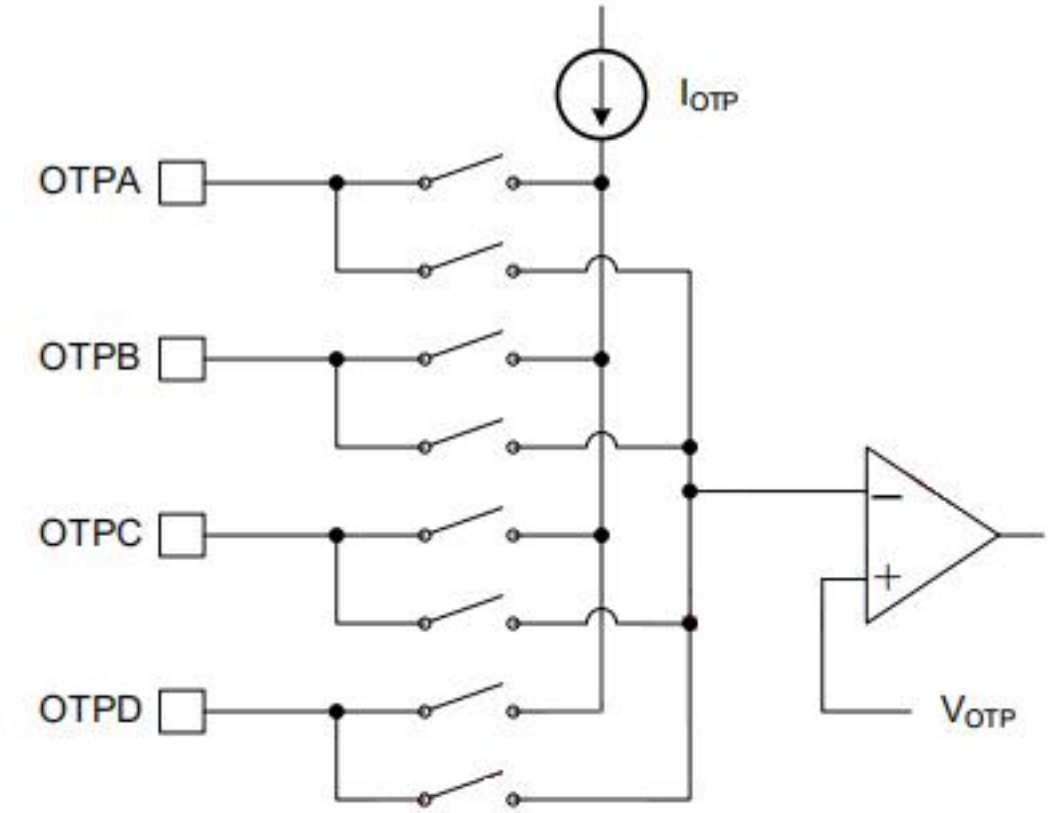


Figure 3.8.3 Schematic Diagram of External Temperature Sensing Component

3.9 On-Chip Temperature Sensing

The chip integrates an on-die temperature sensing circuit. The temperature data read by the MCU is then evaluated to determine whether to trigger over-temperature protection (OTP), depending on the specific application requirements.

3.10 ADC Analog-to-Digital Converter

The on-chip analog-to-digital converter (ADC) features 12-bit resolution and supports more than 20 multiplexed input channels. Specifically, pins P16, P17, GPIO ports C through F, GPIO ports H through K, as well as the ISP and ISN pins, can all be configured as multiplexed ADC inputs via MCU programming.

3.11 Drive signal for the external load switch

An external NMOS power transistor serves as a switch between VCC and VBUS (refer to Section 8, "Typical Application Schematic"). For the switch to turn on, its gate

voltage must be higher than the VCC voltage. The internal charge pump generates a sufficiently high gate voltage to turn on the switch when required.

3.12 GPIO

All GPIO pins can be configured as either inputs or outputs.

3.13 Watchdog Timer

The watchdog timer is used to detect CPU malfunctions, such as software lock-ups caused by noise, voltage interference, or power failure. When its internal counter overflows, it generates a reset signal to reset the CPU.

3.14 Reset Function

The chip provides the following reset signals:

- Power-On Reset (POR)
- 1.8V Regulator Output Under-voltage Reset
- VCC Power Supply Under-voltage Protection (UVLO)
- VDD Under-voltage Reset
- Watchdog Timer Reset
- Program Counter (PC) Overflow Reset

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

at an ambient temperature of 25°C

Parameter	Symbol/Pins	Minimum	Maximum	Units
Voltage range	BST0,BST1,DRH0,DRH1, GATEUSB,GATE1,GATE2	-0.3	30	V
	VSW0,VSW1, VBAT,VBUS,VOUT，PGATEUSB	-0.3	24	V
	CC1, CC2	-0.3	20	V
	DM,DP	-0.3	12	V
	Other I/Os	-0.3	6	V
	DVDD	-0.3	2	V
Junction temperature	T_J		150	℃

Storage temperature	T_{stg}	-40	150	℃
Thermal resistance (junction temperature to environment)	θ_{JA}	29.5		℃/W
Human Body Model	ESD	-2000	2000	V

4.2 Recommended Operating Conditions

Parameter	Symbol/Pins	Minimum	Typical	Maximum	Units
Supply Voltage	VCC,	3		20	V
I/O voltage	CC1, CC2	0	5	5.5	V
Standby power consumption	Istandby			28	uA
Operating temperature	TA	-40		85	℃

4.3 DC Characteristics（Vcc=20V, Operating temperature -20℃ to +105℃）

4.3.1 Power （Vcc, Vdd）

Parameter	Symbol/Pins	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage	VCC		2.8		20	V
VCC supply current (normal operation)	ICC_OPR1	VCC ≥ 4.5V, no load on outputs, MCU operating at16MHz		6		mA
VCC supply current (normal operation)	ICC_OPR2	VCC < 4.5V, no load on outputs,MCU operating at 16MHz		4		mA
Standby current, MCU halted	ICC_STDBY	CC1 or CC2 floating				mA
		CC1 or CC2 connected to a 5.1 kΩ pull-down resistor				mA
VCC Undervoltage Protection (UVP)	VUVLO	VCC rising			2.7	V
		VCC falling	2.6			V
Integrated Regulated Output	VDD		4.75	5	5.25	V

4.3.3 Over-voltage and Under-voltage Protection （OVP, UVLO）

Parameter	Symbol/Pins	Conditions	Minimum	Typical	Maximum	Units
Under-voltage Threshold	UVLO				2.7	V
OVP step size	VOVP_STEP			0.1		V
OVP Threshold Accuracy	ΔVOVP				±5	%
UVP threshold voltage	VUVP				35	V
UVP step size	VUVP_STEP			0.1		V
UVP Threshold Accuracy	ΔVUVP				±5	%

4.3.4 Overcurrent Protection (OCP)

Parameter	Symbol/Pins	Conditions	Minimum	Typical	Maximum	Units
OCP threshold current	IOCP	Rs = 5mΩ, Av = 80	0.5		6.4	A
OCP step size	ΔIOCP	Rs = 5mΩ, Av = 80, IOCP=3.6A		0.1		A

4.3.5 ADC

Parameter	Symbol/Pins	Conditions	Minimum	Typical	Maximum	Units
ADC Accuracy	NADC			12		bit
ADC INL	INLADC	Ta = 25℃, Vin = 2.5V			±5	LSB
ADC DNL	DNLADC	Ta = 25℃, Vin = 2.5V			±5	LSB
ADC Reference Voltage	VREF_ADC	Option 2.56v/4.3v Ta = 25℃, VCC = 5V		2.56		V
				4.3		

4.3.6 CC1, CC2

Parameter	Symbol/Pins	Conditions	Minimum	Typical	Maximum	Units
BMC transmitter high-level output	VOH_CC		1.05	1.125	1.2	V
BMC transmitter low-level output	VOL_CC				0.075	V
BMC Receiver High-Level Input	VIH_CC		0.67		1.45	V
BMC Receiver low-Level Input	VIL_CC		-0.25		0.43	V

BMC transmitter output impedance	ZDriver_CC		33		75	Ω
BMC receiver input impedance	ZBMCRX_CC		1			MΩ
Pull-up current source for CC1/CC2	IRP_CC	0.5A @5V		80		μA
		1.5A @5V		180		μA
		3.0A @5V		330		μA
CC1/CC2 detection threshold voltage	VRd_CC	0.5A @5V		1.6		V
		1.5A @5V		1.6		V
		3.0A @5V		2.6		V

4.3.7 VCONN

Parameter	Symbol/Pins	Conditions	Minimum	Typical	Maximum	Units
VCONN Voltage	VCONN	VCC = 5V, IVCONN = 0mA		4.85		V
		VCC = 5V, IVCONN = 30mA		3.39		V

4.3.8 USB D+ and D- lines

Parameter	Symbol/Pins	Conditions	Minimum	Typical	Maximum	Units
Data Signal Detection Voltage	VDAT_REF		0.25	0.35	0.4	V
Selectable Output Voltage	VSEL_REF		1.8			V
D+/D- pull-down resistors	RDWN		14.25		24.8	KΩ
Resistor between D+ and D- (for DCP mode)	RDCP_DAT			30	40	Ω

4.3.9 External Temperature Detection

Parameter	Symbol/Pins	Conditions	Minimum	Typical	Maximum	Units
Temperature Detection Current Source	IOTP			20.5		μA

4.3.10 On-Chip Temperature Detection

Parameter	Symbol/Pins	Conditions	Minimum	Typical	Maximum	Units
On-Chip Temperature Sensor Accuracy	TTS				±10	℃

4.3.11 GPIO

Parameter	Symbol/Pins	Conditions	Minimum	Typical	Maximum	Units
Output Low-Level Voltage	VOL_GPIO10m	IOL = 10mA, VDD = 5V ISP, ISN, IFB, VFB, GPIOB, GPIOE-F, GPIOH-K, P16, P17			0.5	V
		IOL = 10mA, VDD = 5V GPIOC, GPIOD, CATH			0.4	V
GPIO Hi-Z Leakage	IZ_GPIO				10	μA
Input High-level Voltage VTHS=0	VIH	ISP, ISN, IFB, VFB, GPIOB, GPIOE-F, GPIOH-K, P16, P17	0.8*VDD		VDD	V
		CATH, GPIOC, GPIOD	0.8*VDD		VCC	V
Input Low-level Voltage VTHS=0	VIL	ISP, ISN, IFB, VFB, GPIOB, GPIOE-F, GPIOH-K, P16, P17 CATH, GPIOC, GPIOD	0		0.2*VDD	V
Input High-level Voltage VTHS=1	VIH	ISP, ISN, IFB, VFB, GPIOB, GPIOE-F, GPIOH-K, P16, P17	0.52*VDD		VDD	V
		CATH, GPIOC, GPIOD	0.52*VDD		VCC	V
Input Low-level Voltage VTHS=1	VIL	ISP, ISN, IFB, VFB, GPIOB, GPIOE-F, GPIOH-K, P16, P17 CATH, GPIOC, GPIOD	0		0.13*VDD	V

4.4 AC Characteristics（Vcc=20V, Temperature Range: -20℃ to +105℃）

4.4.1 Internal Oscillator

Parameter	Symbol/Pins	Conditions	Minimum	Typical	Maximum	Units
Main Oscillator Frequency	Foscm			16		MHz
Low-Frequency Clock Oscillator	Fosca			64		KHZ

4.4.2 USB-PD BMC Transmitter and Receiver

Parameter	Symbol/Pins	Conditions	Minimum	Typical	Maximum	Units
BMC Data Rate	f_{BMC}		270	300	330	KHz
BMC Transmitter Rise	t_{RISE_BMC}		300			ns

Time						
BMC Transmitter Fall Time	t_{FALL_BMC}		300			ns
Time from Last Rising Edge to Drive Termination	t_{HOLD_BMC}		1			μs
Packet-to-Packet Interval	t_{IFG_BMC}		25			μs
Data End to Drive-Off Time	t_{END_EMC}				23	μs
BMC Receiver Bandwidth Limiting Window	t_{RXFTR_BMC}		100			ns
Non-Idle Detection Window	t_{NIDLE_BMC}		12		20	μs
Level transition required to exit the idle state	N_{NIDLE_BMC}		3			
Pulse Width for Logic '1' (BMC Transmitter)	t_{PULSE1_BMC}	Ta = 25℃, Total CC Capacitance = 1010pF, CC Pin Series Resistance = 47Ω	1.4		1.8	μs

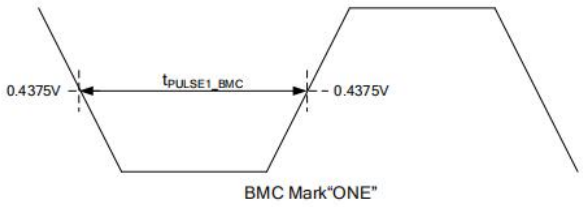


Figure 4.4.2a BMC 时间图

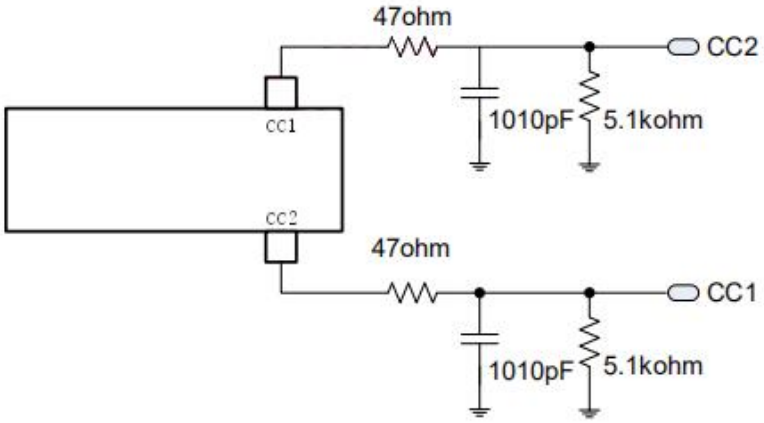
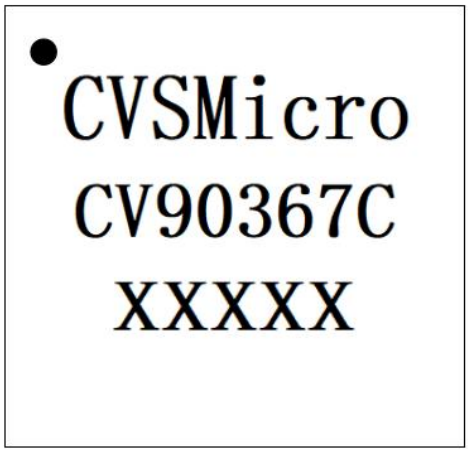


Figure 4.4.2b BMC Transmitter Logic '1' Pulse Width Test Circuit

5 Package Outline

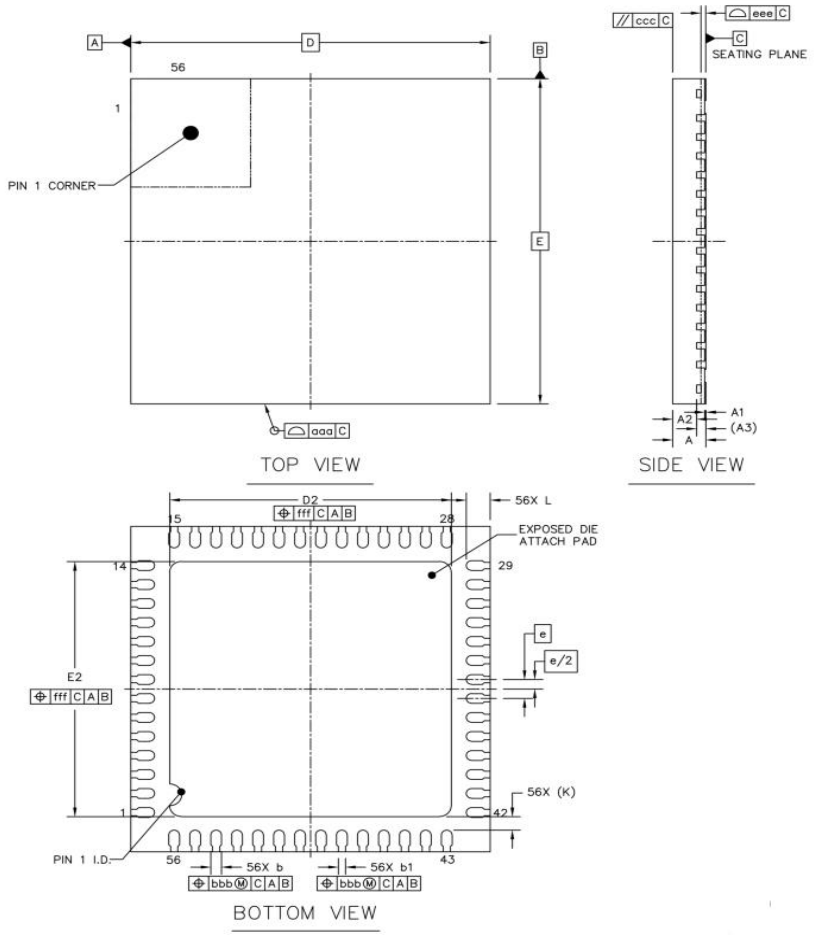
Part Number	Dimension	MSL Rating	Packaging	MPQ
CV90367C	QFN56 (6.00 * 6.00 * 0.85 mm)	MSL 3	Reel	3000 PCS

6 Product Marking Information



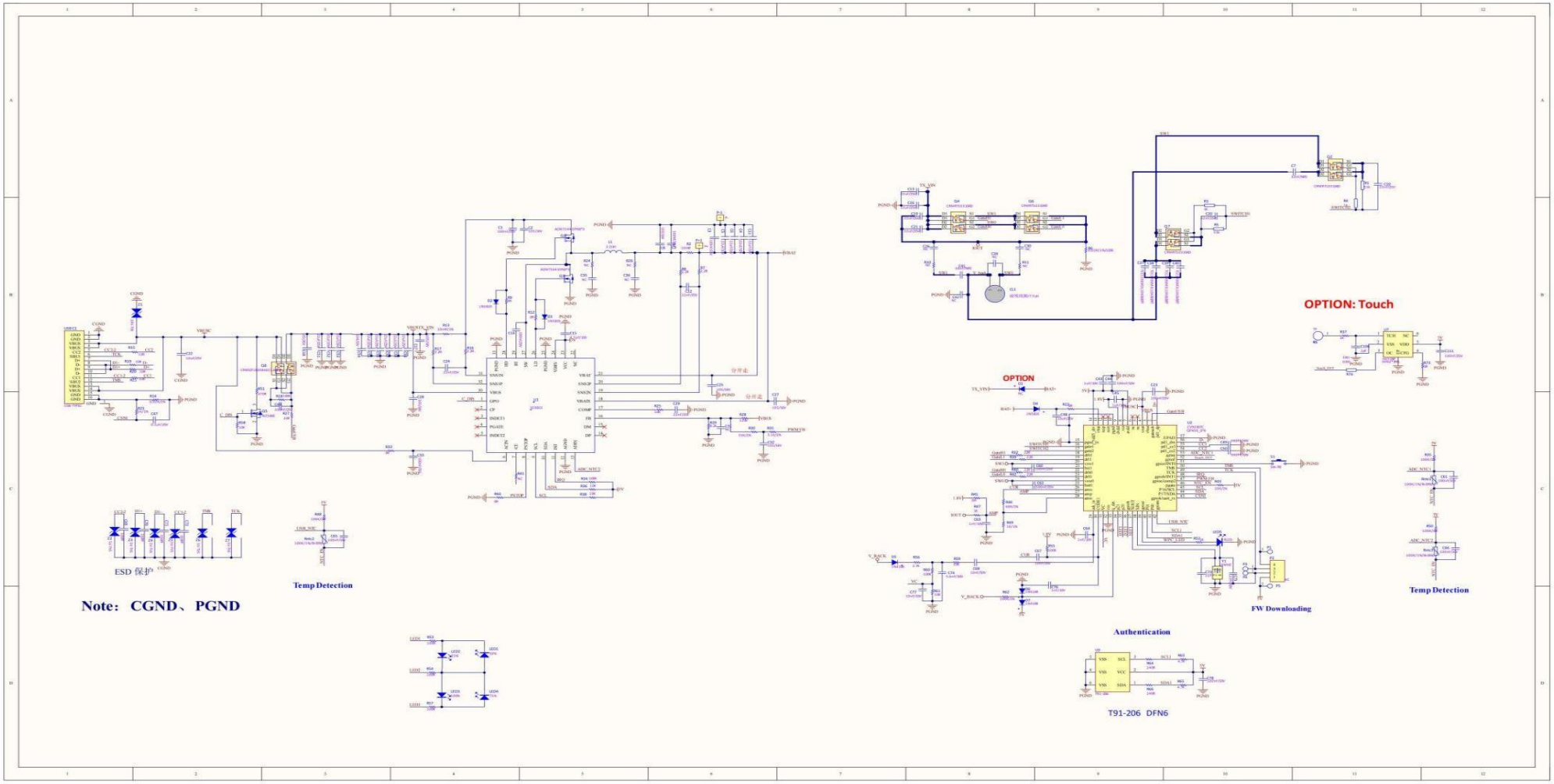
Position	Marking	Description
Line 1	CVSMicro	The Manufacturer
Line 2	CV90367C	The Part Number
Line 3	XXXXX	Lot Number

7 Package Outline Drawing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	-	0.02	0.05
A2	-	0.4	-
A3	0.152REF		
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
D	5.9	6	6.1
E	5.9	6	6.1
D2	4.6	4.7	4.8
E2	4.6	4.7	4.8
e	0.35BSC		
L	0.30	0.40	0.5
K	0.25REF		

8 Qi2.0 Typical Application Circuit



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