Single USB-C Port, Multi- Cell Battery MPP(Qi2.0&Qi2.2)

Wireless Charging Power Bank SOC

1. Description:

CV6057 is a System-on-Chip (SoC) that integrates a USB-C port, battery charge/discharge controller, and wireless charging control circuit. It enables a single-chip solution for single USB-C port, Multi-cell battery magnetic power bank products, significantly saving system cost and board space. Both the battery charge/discharge and wireless charging control circuits integrate pre-drivers capable of directly driving MOSFETs. This structure ensures high system efficiency while allowing flexible layout for optimal PCBA thermal dissipation. The USB-C port supports various input/output fast charging protocols such as PPS/PD/SCP/FCP/QC/AFC/BC1.2.Built-in H-Bridge Synchronous Buck-Boost Controller, 2–5 Cell Li-ion Charge/Discharge Management.It also integrates wireless charging control circuits and pre-drivers, built-in Q-factor detection, communication decoding circuits, FOD detection, and supports Qi protocols including BPP 5W, Apple Magnetic 7.5W, EPP 15W, Qi2.0(MPP 15W), Qi2.2(MPP 25W), etc.

CV6057 offers high integration, rich I/O interfaces, multiple high-precision ADCs, I2C Master and Slave interfaces, and two built-in SPI interfaces, supporting external SPI Flash and TFT image display functions.

CV6057 features low-power design, wide chip operating voltage range (2.8V ~ 5.5V), and USB-C port bidirectional automatic wake-up detection, ensuring extremely low system quiescent power consumption when implementing a wireless charging power bank system with a single chip. Supports Qi value wake-up for wireless charging.

2. Typical Applications

☆ Qi2.0 & Qi2.2 Magnetic Wireless Charging Power Bank.

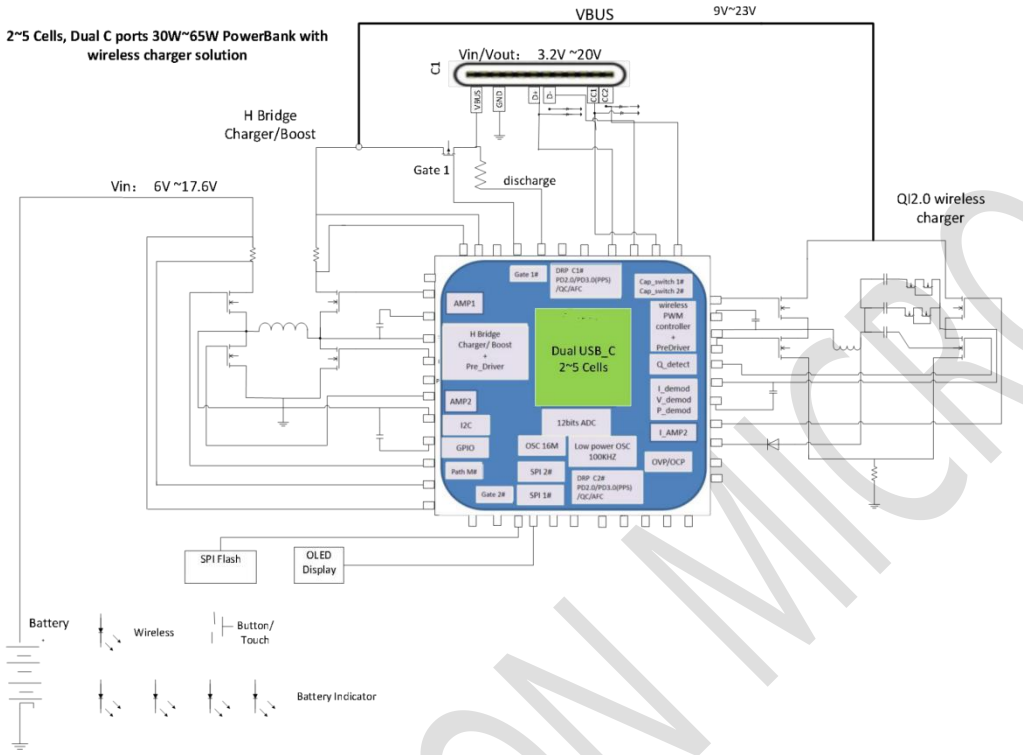
3. Features:

- Operating voltage: 2.8V to 5.5V
- Quiescent current: < 28uA@3.7V
- Built-in 32-bit processor, supports a maximum operating frequency of 48 MHz
- 31 channels of 12-bit high-resolution ADC.
- Built-in H-Bridge Synchronous Boost Controller
- Built-in Full-Featured Wireless Charging Circuit
  - ➢ Q-factor detection

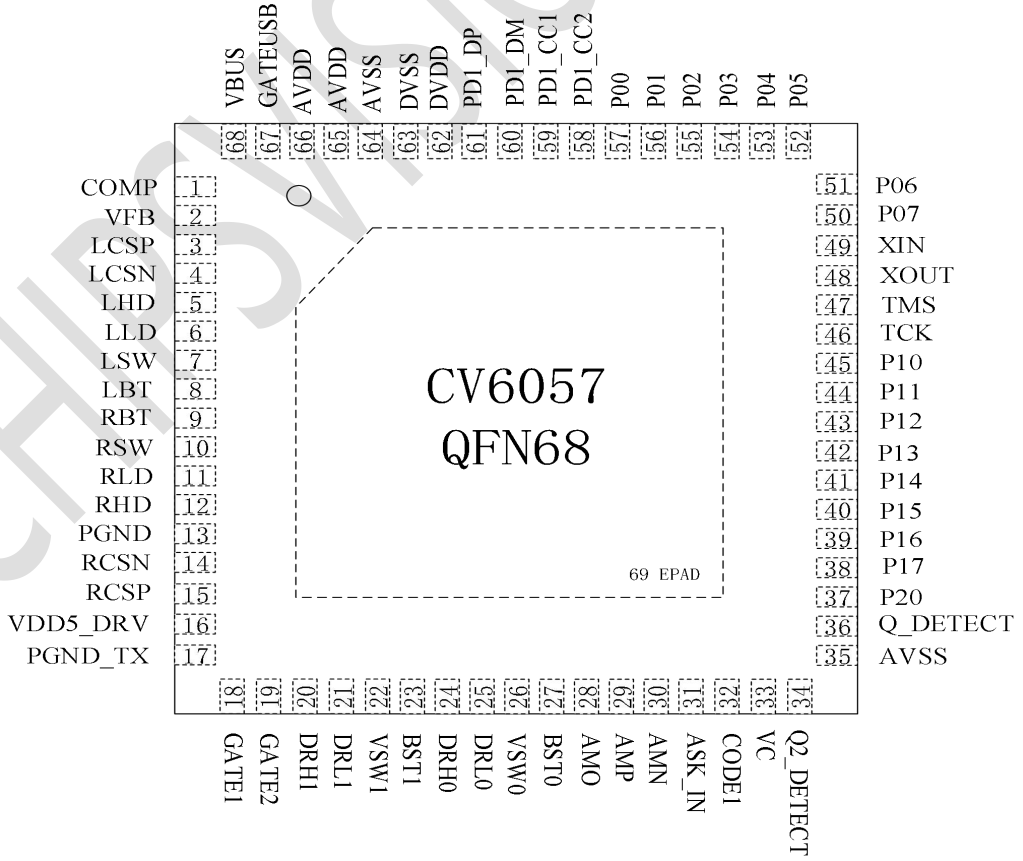
- Current and voltage signal decoding
- The high-speed PWM control circuit includes dead-time control, PWM modulation, and phase-shift control.
- Inverter bridge driver circuit, and high-voltage drive circuit for resonant capacitor switching.
- Foreign Object Detection (FOD),Over-Current Protection (OCP), Over-Voltage Protection (OVP), and Over-Temperature Protection (OTP).

- Built-in I2C master and slave interfaces, and UART, facilitating system daisy-chaining and expansion.
- Built-in two SPI interfaces supporting SPI Flash and graphics display.
- Built-in Dual-Role Port (DRP) fully-featured USB Type-C controller:
  - Supports PD2.0, PD3.0, PD3.1, PD3.2 with PPS.
  - Supports low-power wake-up via CC1, CC2, or DP pins in either direction, as well as GPIO wake-up.
  - Supports fast charging and discharging capabilities.
- Supports multiple fast charging protocol standards
  - Supports PD2.0/PD3.0/PD3.1/PD3.2 (both source and sink roles), including Programmable Power Supply (PPS).
  - Programmable Type-C pull-up resistor/pull-down resistor;built-in VCONN power supply and switch,coordinate E-marker function.
  - Supports QC4.0+/QC3.0/QC2.0
  - Supports AFC
  - Supports FCP
  - Supports SCP
  - Supports BC1.2
  - Supports cable impedance compensation
- Charging Specifications
  - Supports single-cell lithium-ion battery charge and discharge management.
  - Input Voltage Range:VBAT to 24V
- Discharge Specifications
  - Output Voltage:VBAT to 24V
  - Output Current:Up to 5A
  - ingle-Port Output Power Up to 65W
- Battery Level Indication
  - Supports percentage battery level display
  - Support Expandable LED Display
  - Supports 188-segment digital tube display.
  - Supports TFT and OLED graphical displays.
- Wake-up Methods
  - Supports button wake-up
  - Supports USB-C port plug-in wake-up
  - Supports wake-up via touch sensor detection and Q-factor wireless charging detection.
- Multiple protection mechanisms ensuring safety and reliability.
  - Input Under-Voltage and Over-Voltage Protection
  - Input and Output Over-Current Protection
  - Short-Circuit Protection
  - Battery Overcharge, Overdischarge, and Overcurrent Protection.
  - IC Over-Temperature and NTC Over-Temperature Protection
- The system is resilient, flexible, and reduces BOM cost.
- Package Type:QFN68 (7mm X 7mm X 0.75mm).

1 Functional Block Diagram



2 Pin Definitions and Functional Description



Pin	Name	Description
1	COMP	H-Bridge Compensation Pin
2	VFB	H-Bridge Compensation Pin
3	LCSP VOUT	DCDC Current Sense Positive Pin Output Voltage Sense Pin
4	LCSN	DCDC Current Sampling Negative Termina
5	LHD	Buck-Boost H-Bridge Left High-Side Drive Signal
6	LLD	Buck-Boost H-Bridge Left Low-Side Drive Signal
7	LSW	Buck-Boost H-Bridge Left MOSFET Source-Drain Inductor Node
8	LBT	Buck-Boost H-Bridge Left Boost Output
9	RBT	Buck-Boost H-Bridge Right Boost Output
10	RSW	Buck-Boost H-Bridge Right MOSFET Source-Drain Inductor Node
11	RLD	Buck-Boost H-Bridge Right Low-Side Drive Signal
12	RHD	Buck-Boost H-Bridge Right High-Side Drive Signal
13	PGND	Power Ground
14	RCSN VBAT	DCDC Current Sense Negative Pin Battery Voltage Input Pin
15	RCSP	DCDC Current Sense Positive Pin
16	Vdd5_drv	Internal Driver Power Supply
17	Pgnd_tx	Power Ground
18	Gate1	Resonant Capacitor Switch MOSFET Gate Drive
19	Gate2	Resonant Capacitor Switch MOSFET Gate Drive
20	DRH1	High-Voltage Half-Bridge Gate Drive Output, Pin 1
21	DRL1	Low-Voltage Half-Bridge Gate Drive Output, Pin 1
22	VSW1	High-Voltage Half-Bridge Switch Node Connection, Pin 1
23	BST1	High-Voltage Half-Bridge Bootstrap Supply, Pin 1
24	DRH0	High-Voltage Half-Bridge Gate Drive Output, Pin 0
25	DRL0	Low-Voltage Half-Bridge Gate Drive Output, Pin 0

26	VSW0	High-Voltage Half-Bridge Switch Node Connection, Pin 0
27	BST0	High-Voltage Half-Bridge Bootstrap Supply, Pin 0
28	AMO	Operational Amplifier Output
29	AMP	Operational Amplifier Non-Inverting Input (+)
30	AMN	Operational Amplifier Inverting Input (-)
31	ASK_IN	Op-Amp Decoding Input
32	CODE1	Current Decoding Input Pin
33	VC	Over-Voltage Protection (OVP) Input
34	Q2_Detect	Q Factor Detection Input 2
35	AVSS	Ground
36	Q_Detect	Q Factor Detection Input
37	P20	General Purpose Open Drain I/O
38	P17/SDA	General Purpose Open Drain I/O, I2C, clock signal
39	P16/SCL	General Purpose Open Drain I/O, I2C, data signal
40	P15	General Purpose Open Drain I/O
41	P14	General Purpose Open Drain I/O
42	P13	General Purpose Open Drain I/O
43	P12	General Purpose Open Drain I/O
44	P11	General Purpose Open Drain I/O
45	P10	General Purpose Open Drain I/O
46	TCK	Simulation/programming interface clock pin
47	TMS	Simulation/Programming Interface Data Pin
48	XOUT	External Crystal Oscillator Input Pin
49	XIN	External Crystal Oscillator Output Pin
50	P07	General Purpose Open Drain I/O
51	P06	General Purpose Open Drain I/O
52	P05	General Purpose Open Drain I/O
53	P04	General Purpose Open Drain I/O
54	P03	General Purpose Open Drain I/O

55	P02	General Purpose Open Drain I/O
56	P01	General Purpose Open Drain I/O
57	P00	General Purpose Open Drain I/O
58	PD1_CC2	Type-C PD1_CC2 detection pin
59	PD1_CC1	Type-C PD1_CC1 detection pin
60	PD1_DM	Connect the USB port DM
61	PD1_DP	Connect the USB port DP
62	DVDD	Digital section power supply pin: 1.8V
63	DVSS	Ground
64	AVSS	Ground
65	AVDD	5V Power Supply Pin
66	AVDD	5V Power Supply Pin
67	Gateusb	USB port NMOS switch control, built-in boost driver
68	VBUS	VBUS Voltage Sense Pin
69	EPAD	Ground

3 Feature Description

3.1 CPU and Memory

Built-in 32-bit high-performance RISC architecture MCU with 48KB MTP program memory and 7KB SRAM data memory. The device incorporates a 64kHz low-frequency oscillator and a 16MHz high-speed RC main clock oscillator, along with an integrated PLL circuit. The PLL supplies a 48MHz clock to the 32-bit CPU and provides a clock of up to 192MHz for the 16-bit high-speed PWM, ensuring precise frequency variation, pulse-width modulation, and phase shift control in wireless charging applications. A watchdog timer circuit is also integrated.

3.2 USB Type C and PD

3.2.1 USB Type-C Bus Termination and Detection

The source termination resistor (Rp) is implemented by a configurable current source to advertise power capabilities. Attachment/detection is achieved using multiple comparators with different threshold voltages to comply with the Type-C specification.The chip integrates a configurable pull-down resistor (Rd).

When the device operates as a sink, the pull-up resistor (Rp) can be disabled and the pull-down resistor (Rd) enabled. The pull-down resistor is enabled by default upon power-up.

When configured as a source, the Type-C interface enables the pull-up resistor (Rp) and sets the corresponding current level to advertise its power capability.

In Dual-Role Power (DRP) mode, the port alternates between pull-up and pull-down configurations, monitoring the CC1/CC2 pins to determine the sink or source role.Once in low-power mode, the Type-C interface automatically performs attachment detection and wakes up the MCU.

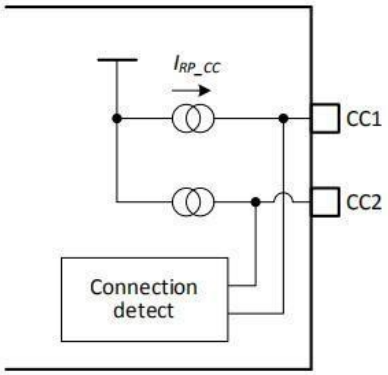


Figure 3.2.1

3.2.2 VCONN

The VCONN supply is switched through an internal MOSFET to deliver power from VDD to the E-Marker cable, with a maximum output of 100 mW. The VCONN switch is controlled by the on-chip MCU and can be turned off after the E-Marker cable is detected to reduce power consumption.

3.2.3 USB BC1.2 、QC3.0、QC4.0

The chip is compliant with the USB Battery Charging Specification Revision 1.2 and supports the High Voltage Dedicated Charging Port (HVDCP) QC3.0 protocol. HVDCP utilizes signaling compatible with USB BC1.2 on the D+ and D- lines to negotiate voltage requests on VBUS. QC3.0 is backward compatible with Quick Charge 1.0 and 2.0. Quick Charge 3.0 offers finer voltage increments from 3.6V to 20V in 200mV steps.

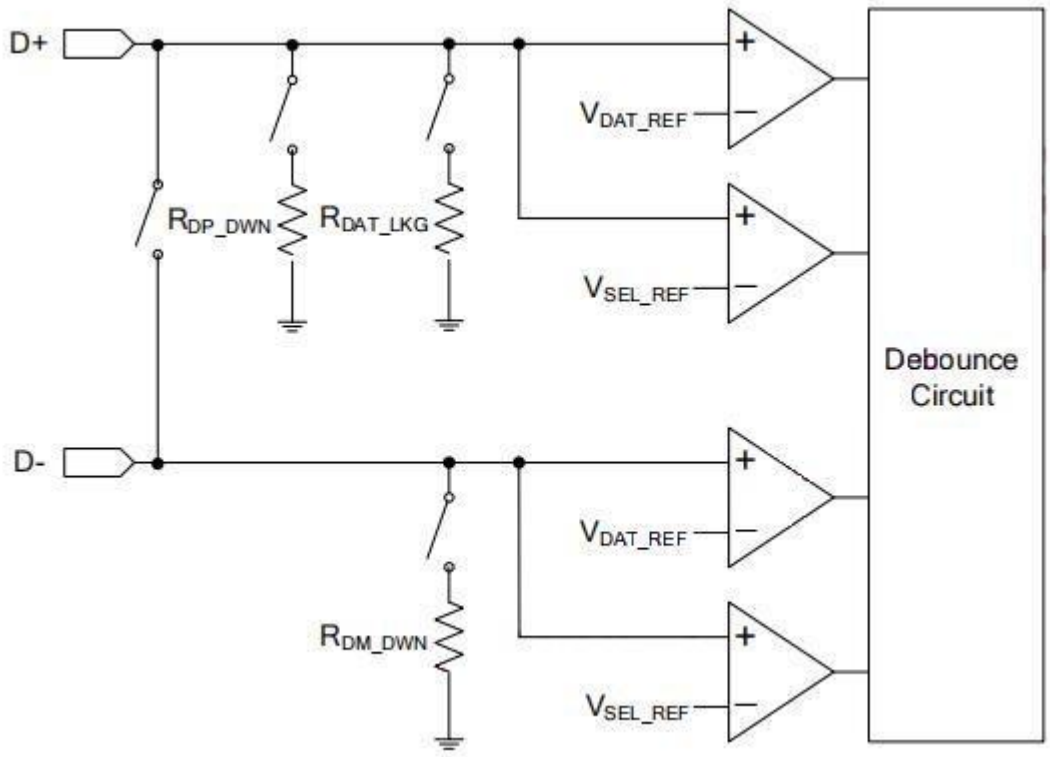


Figure 3.2.3 Internal Circuit Diagram of USB Interface D+ and D- Lines

3.3 H-Bridge Synchronous Buck-Boost (Charge/Discharge)

3.3.1 Functional Description of the Charge/Discharge Circuit

The CV6057 integrates a hardware battery charge/discharge controller and MOSFET drivers. It supports peak current detection and features a hardware triangle-wave generator, with an operating frequency configurable from 200kHz to 800kHz. The device incorporates input voltage feedforward and comprehensive protection mechanisms, including Undervoltage Lockout (UVLO), Overvoltage Protection (OVP), Overcurrent Protection (OCP), Short-Circuit Protection (SCP) with alarm, and Overtemperature Protection (OTP). It supports a complete charging cycle management: Trickle Charge, Constant Current (CC) Charge, and Constant Voltage (CV) Charge. The battery termination voltage is software-configurable, supporting charging for various battery types such as 4.2V, 4.35V, 4.4V, and 4.5V batteries. Additionally, it supports a high-efficiency boost discharge mode with an output voltage of up to 24V.

3.4 Buck-Boost DC-DC Converter

3.4.1 Buck-Boost DC-DC Converter typically includes the following configurations:

- Configurable Buck-Boost and Charge/Discharge Operating Modes
- The output voltage is adjustable from VBAT to 24V with a resolution of 20mV.
- High-side current sensing module, to provide constant current and short-circuit current protection.
- Output Overvoltage Protection (OVP)
- Supports an operating frequency range from 200kHz to 800kHz, configurable via software or external resistor.
- Supports bidirectional operation in buck-boost mode
- Selectable driver dead-time for efficiency control.
- Selectable DC-DC control ramp top and bottom voltages for output range adjustment.

3.5 Wireless Charging

3.5.1 H-Bridge PWM Control

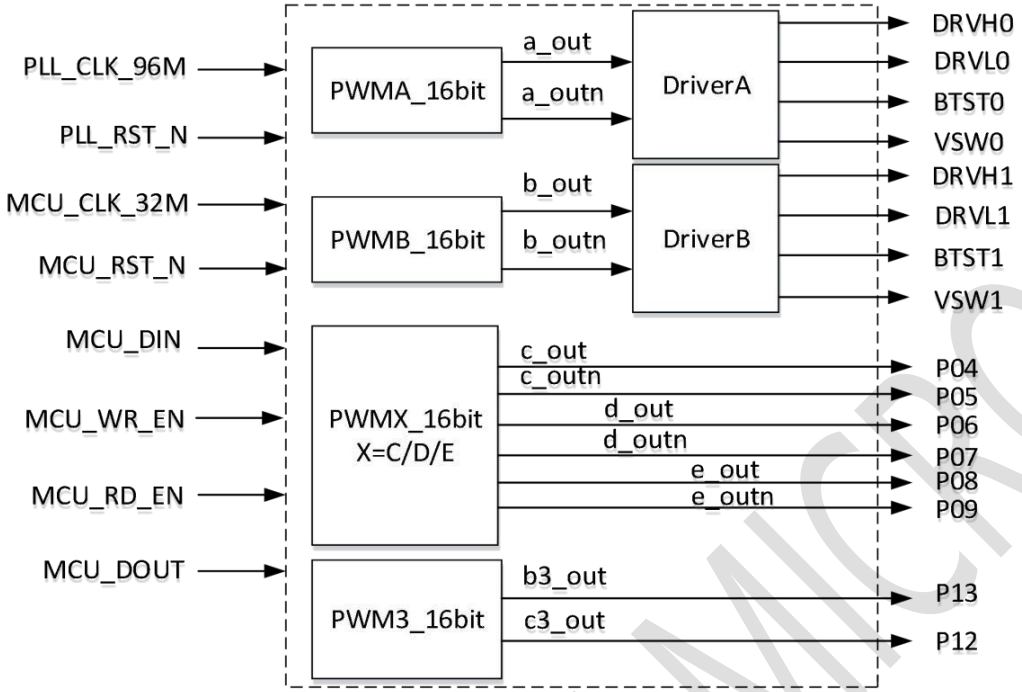


Figure 3.5.1 Full-Bridge PWM Control Diagram

The PWM module operates at a frequency of 156 MHz and integrates five PWM output channels, labeled A through E. Channels A and B form a complementary pair (i_OUT and i_OUTN), as do C and D, while channel E is a single-ended output. Channels A and B each have a dedicated internal driver (Driver A and Driver B, respectively).

Feature Description：

- For each output channel (A/B, C/D, and E), the PWM module provides a 16-bit up-counting auto-reload counter, 16-bit programmable registers for period and duty cycle, and an 8-bit dead-time register.
- Allows the timer registers to be updated after a specified number of counter cycles and repeats the counting process.
- The PWM outputs can be configured to form three independent full-bridge circuits through the pairs A/B, C/D, and A/C. Each bridge operates independently yet remains synchronized with the others, supporting phase shifting, pulse-width modulation, and dead-time adjustment. (Note: The A/C pair can also be configured as a full-bridge.)

- When configured as a full-bridge pair, channels A and B share the same period and duty-cycle settings while utilizing independent dead-time registers.Channel B's output is phase-shifted with reference to Channel A.

- When configured as an A/C full-bridge pair, Channels A and C share the period and duty cycle settings (based on Channel A's registers) but utilize independent dead-time configurations. The output of Channel C is phase-shifted relative to Channel A. In this mode, Channel C multiplexes the hardware resources normally assigned to Channel B, allowing Channel D to remain operational independently.

- When configured as a full-bridge pair, Channels C and D share the period and duty cycle settings (based on Channel C's registers) while utilizing independent dead-time configurations. The output of Channel D is phase-shifted relative to Channel C.

- Channels A, B, and C can be configured to provide four complementary PWM outputs.
  - Share the A_COUNT counter and period register from Channel A.
  - Duty cycle and dead time are configured independently for each channel.
  - The hardware resources of Channel C are multiplexed to Channel D.
- Brake Input with hardware and software brake support.
- Each output pair (i_OUT/i_OUTN) has its own independent output enable control.
- Supports real-time updates to period, duty cycle, dead time, and 360-degree phase shift registers, ensuring the integrity of the PWM cycle.

PWM3_16BIT consists of two independent 16-bit PWM output channels: B3_OUT and C3_OUT.

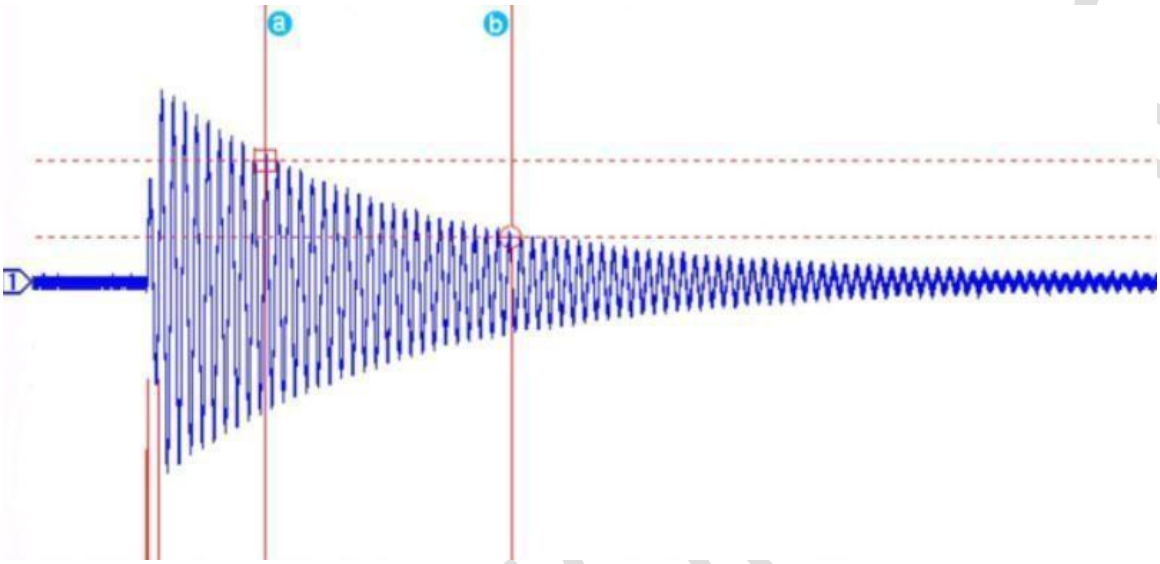
PWM3_16BIT includes a 16-bit auto-reload counter named A_COUNT.

Feature Description：

- Basic Timing.
- Supports simultaneous drive of two independent PWM output channels.

3.6 Q-factor Description

Switch on the high side transistor of the half bridge. Let the LC tank circuit to charge up to a specific energy level before turning on the low side transistor of the half bridge. The LC circuit will then resonate at a high frequency which amplitude decays exponentially.



3.7 Analog ping

The CV6057 sends a short pulse to the LC tank to initiate oscillation. When an RX (receiver) is present, the oscillation amplitude changes, enabling RX detection. This Analog Ping function significantly reduces the average standby power consumption of the TX (transmitter).

3.8 硬件过压保护

CV6057 incorporates a hardware over-voltage protection (OVP) circuit. This enables the chip to implement a fast-triggering protection mechanism, preventing excessive resonant voltage on the coil due to abnormal conditions (such as the presence of a foreign object) from subjecting transmitter system components and the receiving device to high-voltage stress. CV6057 features a triple-stage over-voltage protection mechanism. First Stage: Software Protection， When the VC voltage reaches or approaches a software-preset protection threshold, the software stops increasing the transmitted energy. When the divided voltage from VC (via resistors R1/R2) exceeds the voltage at the comparator's inverting input (3.3V), the hardware protection mechanism is triggered. The OVP signal generates a "Half Bridge Lock" signal, which

locks the full-bridge operating mode into a half-bridge mode (Q3 is turned off and Q4 remains constantly on). In this mode, the transmission energy is halved, and an OVP interrupt is generated. If communication between the transmitter (TX) and receiver (RX) remains normal and the VC voltage does not continue to rise, the software can decide whether to resume normal charging. If the VC voltage continues to rise even in half-bridge mode, the system triggers the third protection stage: turning off Q1 and Q3 while keeping Q2 and Q4 MOSFET constantly on, causing the system to enter a discharge state.

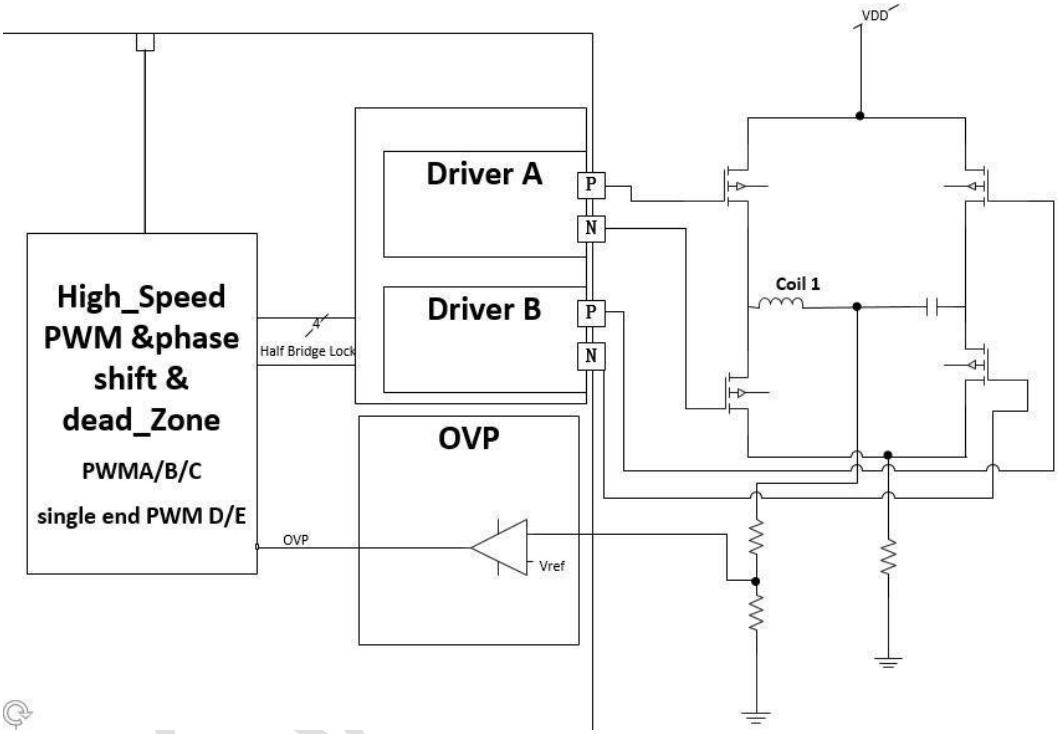


Figure 3.8.1 Hardware Protection circuit Block Diagram

3.9 Foreign Object Detection

The CV6057 utilizes a dual-method approach (Q-factor detection and power loss detection) for Foreign Object Detection (FOD), enabling accurate, rapid judgment and protection:Q-factor Detection：If the Q-factor detected by the transmitter (TX) is lower than the preset threshold, an FOD alarm is triggered immediately.Power Loss Detection：The CV6057 integrates a high-precision ADC. If the difference between the TX transmitted power and the RX received power exceeds a preset threshold, the system makes an accurate determination and triggers FOD protection.

3.10 Protection Circuit

3.10.1 OVP and UVP

As shown in Figure 7.10.1, the VCC voltage is compared against a reference voltage generated by the DAC to produce over-voltage (OV) and under-voltage (UV) signals. Simultaneously, the MCU is interrupted, and the control signal (GATE) for the external load switch is removed, turning off the load switch.

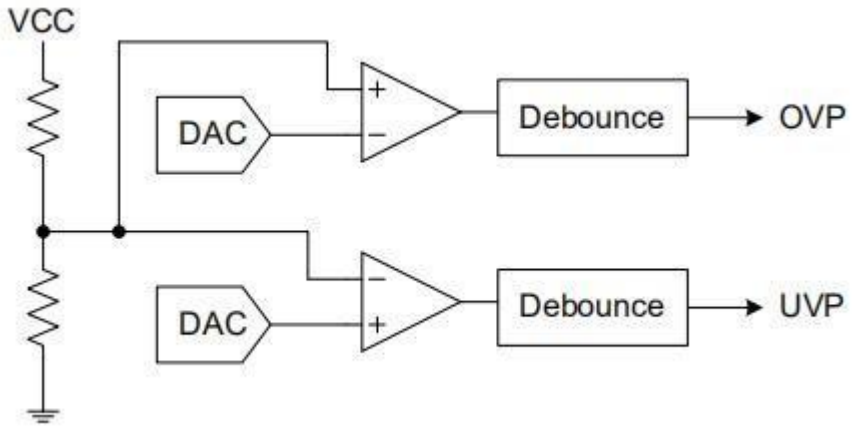


Figure 3.10.1

3.10.2 Over-current Protection

The load current signal is amplified by the current sense amplifier and then digitized by the ADC. Both the over-current trigger threshold and the shaking time are configurable via firmware.

3.10.3 Over-Temperature Protection

The external over-temperature protection for the chip is implemented using a constant current source and a voltage comparator. The current source outputs to an external pin, generating a voltage drop across an NTC thermistor. When this voltage falls below the internally set reference voltage (V_OTP), the comparator output triggers an alarm: the GATE signal is disabled and an interrupt is sent to the MCU. The voltage at this pin can also be measured by the ADC.

Select an NTC thermistor with a B-value of 4100K and a nominal resistance of either 200 kΩ or 100 kΩ for the over-temperature protection circuit. The protection trigger point is configurable to 95°C, 105°C, 115°C, or 125°C.

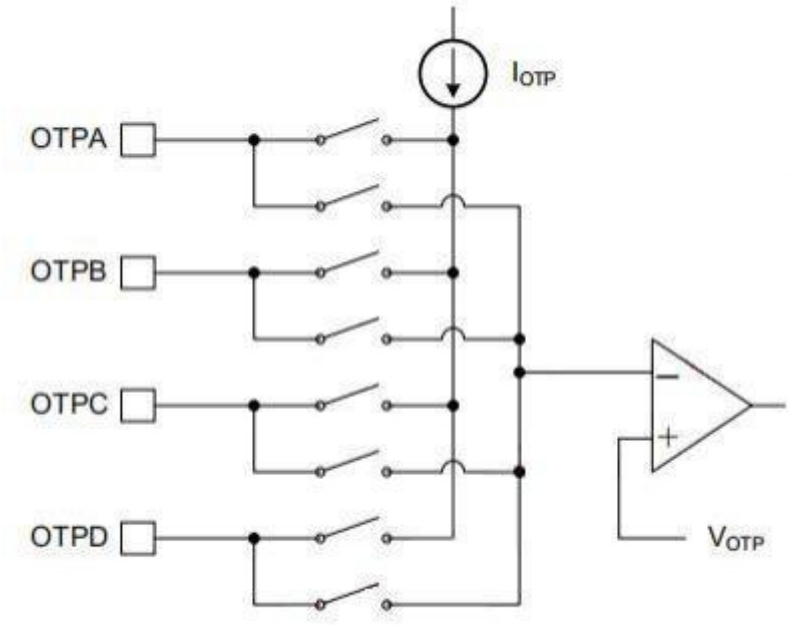


Figure 3.10.3 Schematic Diagram of External Temperature Sensing Component

3.11 On-Chip Temperature Sensing

The chip integrates an on-die temperature sensing circuit. The temperature data read by the MCU is then evaluated to determine whether to trigger over-temperature protection (OTP), depending on the specific application requirements.

3.12 ADC Analog-to-Digital Converter

The on-chip analog-to-digital converter (ADC) features 12-bit resolution and supports more than 20 multiplexed input channels. Specifically, pins P16, P17, GPIO ports C through F, GPIO ports H through K, as well as the ISP and ISN pins, can all be configured as multiplexed ADC inputs via MCU programming.

3.13 Drive signal for the external load switch

An external NMOS power transistor serves as a switch between VCC and VBUS (refer to Section 7, "Typical Application Schematic"). For the switch to turn on, its gate voltage must be higher than the VCC voltage. The internal charge pump generates a sufficiently high gate voltage to turn on the switch when required.

3.14 GPIO

All GPIO pins can be configured as either inputs or outputs.

3.15 Watchdog Timer

The watchdog timer is used to detect CPU malfunctions, such as software lock-ups caused by noise, voltage interference, or power failure. When its internal counter overflows, it generates a reset signal to reset the CPU.

3.16 Reset Function

The chip provides the following reset signals:

- Power-On Reset (POR).
- 1.8V Regulator Output Under-voltage Reset.
- VCC Power Supply Under-voltage Protection (UVLO).
- VDD Under-voltage Reset.
- Watchdog Timer Reset.
- Program Counter (PC) Overflow Reset.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Voltage range	BST0，BST1，DRH0，DRH1 GATEUSB，GATE1，GATE2,LHD RHD,LBT,RBT,VBUS RCSN,RCSP,LCSP,LCSN	-0.3	30	V
	VSW0,VSW1,LSW,RSW	-0.3	24	V
	PD1_CC1,PD1_CC2	-0.3	20	V
	PD1_DM, PD1_DP	-0.3	12	V
	DVDD,XIN,XOUT	-0.3	2	V

	AVSS,VSS,DVSS,PGND,PGND_TX	-0.3	0.3	V
	Other Pins	-0.3	6	V
Junction temperature	T_J		150	℃
Storage temperature	T_{stg}	-40	150	℃
Human Body Model	ESD	-2000	2000	V

4.2 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply Voltage	VCC	2.8		28	V
I/O voltage	CC1, CC2	0	5	5.5	V
Standby power consumption	$I_{standby}$			28	uA
Operating temperature	T_A	-40		85	℃

4.3 Power Characteristics（Operating temperature -20℃ to +105℃）

4.3.1 Power （Vcc, Vdd）

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
VCC supply current (normal operation)	ICC_OPR1	VCC ≥ 4.5V, no load on outputs, MCU operating at10MHz		7		mA
VCC supply current (normal operation)	ICC_OPR2	VCC < 4.5V, no load on outputs,MCU operating at 10MHz		4		mA
Standby current, MCU halted	ICC_STDBY	CC1 or CC2 floating				mA
		CC1 or CC2 connected to a 5.1 kΩ pull-down resistor				mA
VCC Undervoltage Protection (UVP)	VUVLO	VCC rising			2.85	V
		VCC falling	2.6			V
Integrated Regulated Output	VDD		4.75	5	5.25	V

4.3.2 Shunt Regulator

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Voltage Tolerance （Figure 4.3.2）	VOUT	VPWR=23V， Ta=25C, 5V Output			±1.5	%
		VPWR=23V, Ta=25C, 3V ~ 21V Output			±2.5	%
		VPWR=23V, Ta=-20C - 105C, 3V ~ 21V Output			±3.5	%
PPS Voltage Step	Vpps_step	R_{SENSE}=5mΩ, Av=80		20		mV
PPS Current Limit Step	Ipps_step	R_{SENSE}=5mΩ, Av=80		50		mA
Current Limit Tolerance	ΔIPPS_CL	1A ≤ Current Limit Value ≤ 3A			±150	mA
		Current Limit Value>3A			±5	%

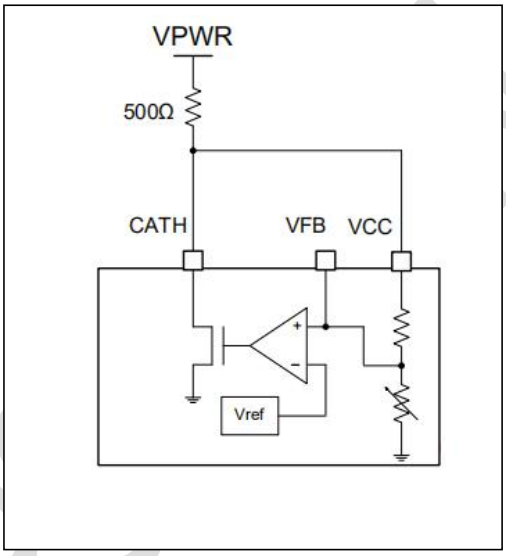


Figure 4.3.2 Test Circuit for the Shunt Regulator

4.3.3 Overvoltage and Undervoltage Protection （OVP, UVLO）

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Undervoltage Trigger Point	UVLO				3	V
OVP Step	VOVP_STEP			0.1		V
OVP Threshold Accuracy	ΔVOVP				±5	%
UVP Voltage Threshold	VUVP				35	V
UVP Step	VUVP_STEP			0.1		V
UVP Threshold Accuracy	ΔVUVP				±5	%

4.3.4 Overcurrent Protection (OCP)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
OCP threshold current	IOCP	Rs = 5mΩ, Av = 80	0.5		6.4	A
OCP step	ΔIOCP	Rs = 5mΩ, Av = 80, IOCP=3.6A		0.1		A

4.3.5 ADC

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
ADC Accuracy	NADC			12		bit
ADC INL	INLADC	Ta = 25℃, Vin = 2.5V			±5	LSB
ADC DNL	DNLADC	Ta = 25℃, Vin = 2.5V			±5	LSB
ADC Reference Voltage	VREF_ADC	Option 2.56v/4.3v Ta = 25℃, VCC = 5V		2.56		V
				4.3		

4.3.6 CC1, CC2

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
BMC transmitter high-level output	VOH_CC		1.05	1.125	1.2	V
BMC transmitter low-level output	VOL_CC				0.075	V
BMC Receiver High-Level Input	VIH_CC		0.67		1.45	V
BMC Receiver low-Level Input	VIL_CC		-0.25		0.43	V
BMC transmitter output impedance	ZDriver_CC		33		75	Ω
BMC receiver input impedance	ZBMCRX_CC		1			MΩ
Pull-up current source for CC1/CC2	IRP_CC	0.5A@5V		80		μA
		1.5A@5V		180		μA
		3.0A@5V		330		μA
CC1/CC2 detection threshold voltage	VRd_CC	0.5A@5V		1.6		V
		1.5A@5V		1.6		V
		3.0A@5V		2.6		V

4.3.7 VCONN

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
VCONN Voltage	VCONN	VCC = 5V, IVCONN = 0mA		4.85		V
		VCC = 5V, IVCONN = 30mA		3.39		V

4.3.8 USB_D+/D- lines

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Data Signal Detection Voltage	VDAT_REF		0.25	0.35	0.4	V
Selectable Output Voltage	VSEL_REF		1.8			V
D+/D- pull-down resistors	RDWN		14.25		24.8	KΩ
Resistor between D+ and D- (for DCP mode)	RDCP_DAT			30	40	Ω

4.3.9 External Temperature Detection

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Temperature Detection Current Source	IOTP			20.5		μA

4.3.10 On-Chip Temperature Detection

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
On-Chip Temperature Sensor Accuracy	TTS				±10	℃

4.3.11 GPIO

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Low-Level Voltage	VOL_GPIO10m	IOL = 10mA, VDD = 5V ISP, ISN, IFB, VFB, GPIOB, GPIOE-F, GPIOH-K, P16, P17			0.5	V
		IOL = 10mA, VDD = 5V GPIOC, GPIOD, CATH			0.4	V
GPIO Hi-Z Leakage	IZ_GPIO				10	μA
Input High-level Voltage VTHS=0	VIH	ISP, ISN, IFB, VFB, GPIOB, GPIOE-F, GPIOH-K, P16, P17	0.8*VDD		VDD	V

		CATH, GPIOC, GPIOD	0.8*VDD		VCC	V
Input Low-level Voltage VTHS=0	VIL	ISP, ISN, IFB, VFB, GPIOB, GPIOE-F, GPIOH-K, P16, P17 CATH, GPIOC, GPIOD	0		0.2*VDD	V
Input High-level Voltage VTHS=1	VIH	ISP, ISN, IFB, VFB, GPIOB, GPIOE-F, GPIOH-K, P16, P17	0.52*VDD		VDD	V
		CATH, GPIOC, GPIOD	0.52*VDD		VCC	V
Input Low-level Voltage VTHS=1	VIL	ISP, ISN, IFB, VFB, GPIOB, GPIOE-F, GPIOH-K, P16, P17 CATH, GPIOC, GPIOD	0		0.13*VDD	V

4.3.12 DC-DC Buck-Boost Converter

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output Voltage Level	Vout_sel	Iout = 1mA	3.2		34	V
Maximum OVP Threshold	Ovp_rise	Vout > 理想值，触发过压	112.5		120	%
Minimum OVP Threshold	Ovp_fall	Vout < 理想值，回复正常	90		100	%

4.4 AC Characteristics（Vcc=20V, Temperature Range: -20℃ to +105℃）

4.4.1 Internal Oscillator

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Main Oscillator Frequency	Foscm			16		MHz
Low-Frequency Clock Oscillator	Fosca			64		KHZ

4.4.2 USB-PD BMC Transmitter and Receiver

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
BMC Data Rate	f_{BMC}		270	300	330	KHz
BMC Transmitter Rise Time	t_{RISE_BMC}		300			ns
BMC Transmitter Fall Time	t_{FALL_BMC}		300			ns
Time from Last Rising Edge to Drive Termination	t_{HOLD_BMC}		1			μs
Packet-to-Packet	t_{IFG_BMC}		25			μs

Interval						
Data End to Drive-Off Time	t_{END_EMC}				23	μs
BMC Receiver Bandwidth Limiting Window	t_{RXFTR_BMC}		100			ns
Non-Idle Detection Window	t_{NIDLE_BMC}		12		20	μs
Level transition required to exit the idle state	N_{NIDLE_BMC}		3			
Pulse Width for Logic '1' (BMC Transmitter)	t_{PULSE1_BMC}	Ta = 25℃, CC 总电容 = 1010pF, CC 管脚串联电阻 = 47Ω	1.4		1.8	μs

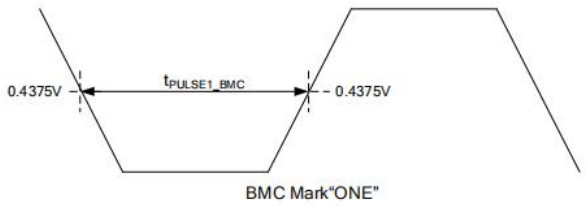


Figure 4.4.2a BMC Timing Diagram

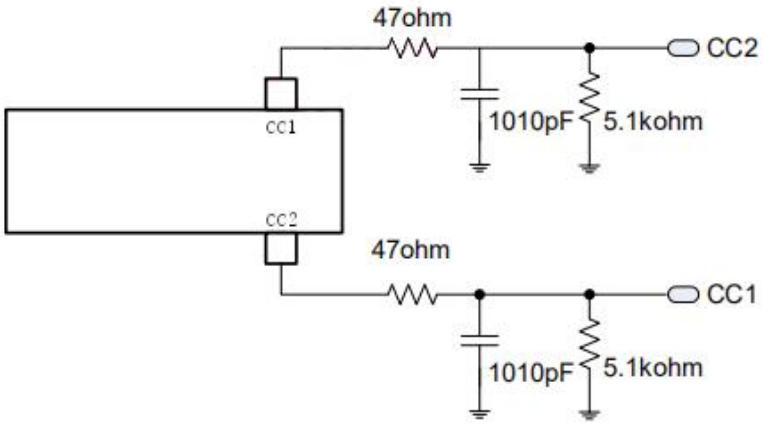


Figure 4.4.2b BMC Transmitter Logic '1' Pulse Width Test Circuit

4.4.3 DC-DC Buck-Boost Converter

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Switching Frequency	fdcdc		190	390	755	KHz
Drive Dead Time	Driver_dt		39		140	ns
Debounce Delay	debounce		100		200	ns

5 Package Outline

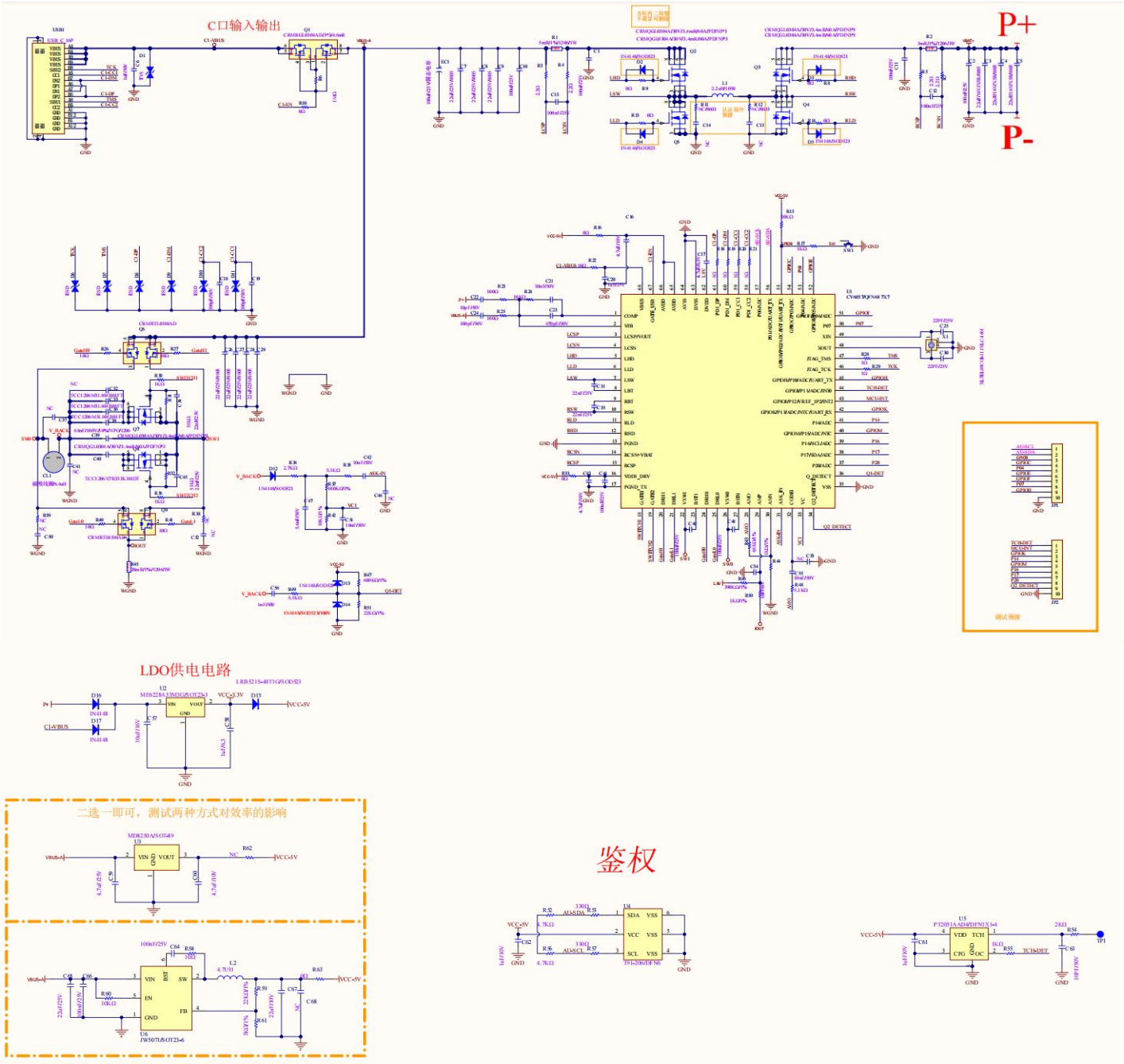
Package outline drawing on page 26 of this document.

Part Number	Package	MSL Rating	Packaging	MPQ
CV6057	QFN68 （7.00 * 7.00 * 0.75 mm）	Level 3	Reel	3000 PCS

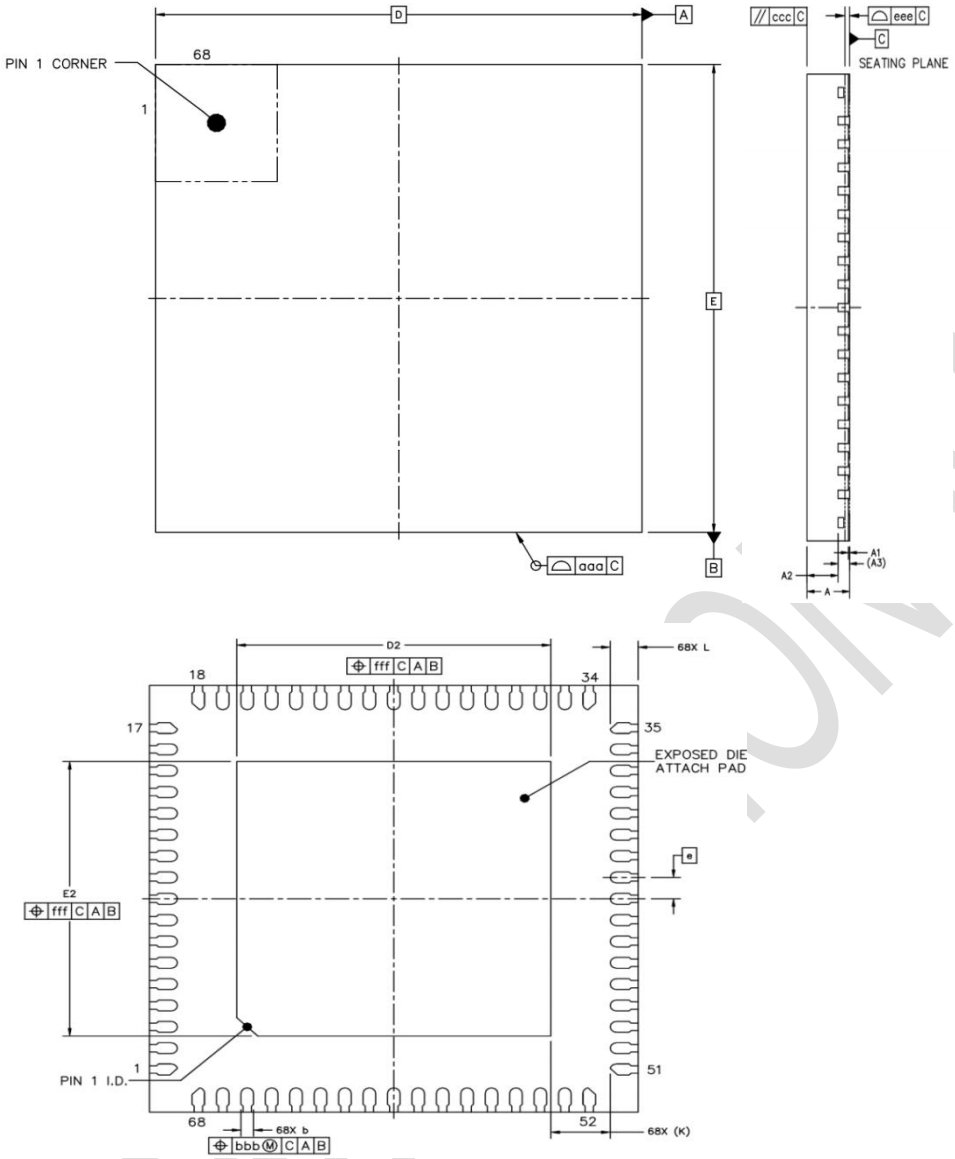
6 Product Marking

Position	Marking Content	Meaning
Line 1	CVSMicro	Company logo
Line 2	CV6057	The part number
Line 3	XXXXX	Lot Number

7 Application schematic diagram



8 Package Outline Drawing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
A2	-	0.55	-
A3	0.203REF		
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
D	6.9	7	7.1
E	6.9	7	7.1
D2	4.4	4.5	4.6
E2	4.4	4.5	4.6
e	0.35BSC		
L	0.30	0.40	0.5
K	0.85REF		

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