

A wireless charging transmitting SoC that supports Qi2.2 standards

1 Description

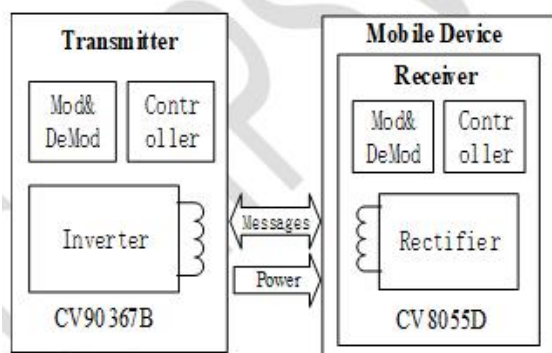
The CV90367B is a wireless charging transmitter system-on chip (SoC), which supports various types of power supply adapters such as PD2.0 PD3.0, QC2.0, QC3.0, AFC. CV90367B supports the latest Qi V1.2, Qi V1.3 and Qi 2.2 versions, single-coil/multi-coil wireless charging applications, diversified charging specifications such as BPP5W, Apple 7.5W, Samsung PPDE 10W, EPP 15W, MPP 15W MPP 25W profiles. Supports customer-proprietary protocols with power up to 80W.

The CV90367B has Integrated under-voltage protection, hardware over-voltage protection, over-current protection, over-temperature protection and other functions. It also supports Q value and FOD detection.

Integrates with the full-bridge drive circuit as well as voltage and current communication decoding function module, CV90367B adopts QFN48 package to significantly reduce PCB size and save BOM cost.

2 Typical Applications

- ☆ Standard, High power wireless charging base
- ☆ Automotive wireless charging devices
- ☆ Mobile power wireless charging equipment



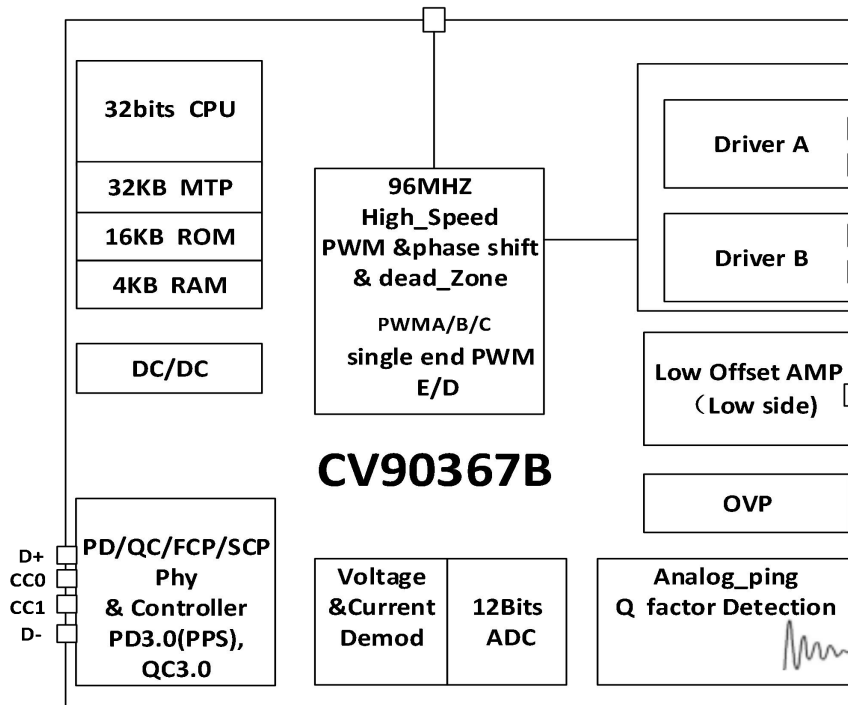
3 Features

- In compliance with Qi V1.2, QiV1.3 and Qi2.2 standards
- Supports Qi standard BPP 5W, Apple 7.5W, Samsung PPDE 10W, EPP 15W, MPP15W, MPP 25W charging; supports customer-proprietary protocols with power up to 80W
- Integrated 32-bit high-speed CPU core
- Integrated 32 KB MTP, 16 KB Mask ROM and 4 KB RAM; supports FW upgrade via Type-C port
- Supports multiple fast-charging protocols including PD2.0, PD3.0 PPS, QC2.0, QC3.0, AFC and SCP.
- Integrated full-bridge MOS gate driver
- Built-in 4 pairs of complementary 16-bit high-speed PWM @128 MHz, and 2 channels of independent high-speed 16-bit PWM
- 8 channels of 12-bit high-precision ADC
- Built-in dual-channel decoding for voltage and current
- Built-in low-offset operational amplifier
- Built-in hardware over-voltage protection
- Supports Q-value detection
- Supports FOD (Foreign Object Detection) foreign object detection function
- 11 GPIOs, supporting I2C and UART communication.

4 Product Information

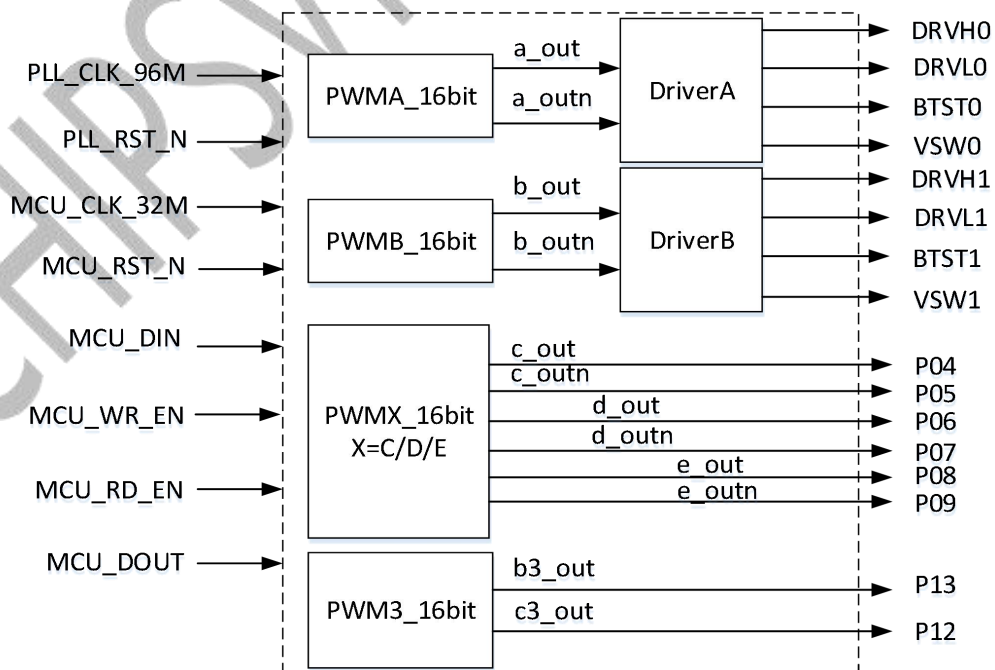
Part Number	Package	Package Size
CV90367B	QFN48	6.00 * 6.00 * 0.75 mm

1 System Block Diagram



2 Functional Description

2.1 Full-bridge control PWM



The PWM is designed with a frequency of 96 MHz and integrated with 5 channels of PWM output, which are A/B, C/D, and E (this article uses i to stand for A/B/C/D/E).

Among them, the complementary output of A, B, and C is i_OUT/i_OUTN, D, and E single-ended output. A and B outputs integrate internal Driver A and Driver B.

Features:

- Each output of A/B, C/D, and E has a 16-bit upward auto-loading counter with a 16-bit configurable period/duty cycle and 8-bit dead zone register;
- It is allowed to update the timer register to repeat the count after a specified number of counter cycles;
- A/B, A/C, and C/D outputs can be combined into a full bridge respectively. Three full-bridge outputs do not interfere with each other. Each group keeps synchronization and supports shift phase, pulse width adjustment, and dead zone. The A/C output can also be combined into a full bridge;
 - A and B outputs form a full bridge, and both share the period and duty cycle of A and use their own dead zones.

B is based on A and supports phase shift;
 - A and C outputs form a full bridge, and both share the period and duty cycle of A and use their own dead zones.

C is based on A and supports phase shift. The resources used by C is those of B. The resources of C can be reused by D and work independently;
 - C and D outputs form a full bridge, and both share the period and duty cycle of C and use their own dead zones.

D is based on C and supports phase shift.
- A, B, and C can form 6 PWM complementary outputs.
 - They share the A_COUNT and period of A;
 - They use own duty cycles and dead zones;
 - The resources of C are used by D;
- Brake input supports hardware brake and software brake;
- Each i_OUT/i_OUTN has its own output enable control;
- Support online dynamic change of period, duty cycle, dead zone and 360-degree phase shift register to ensure the integrity of the period;

PWM3_16BIT is composed of two independent PWM outputs, namely, B3_OUT and

C3_OUT.

PWM3_16BIT is composed of a 16-bit A_COUNT auto-loading counter.

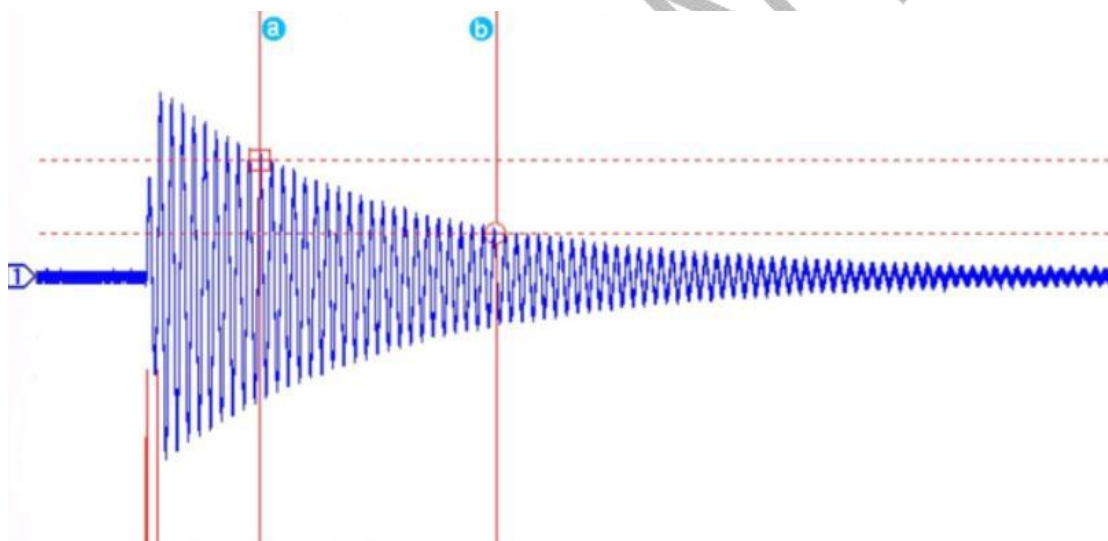
Features:

- Basic timing function;
- Driving 2 PWM waveform outputs at the same time.

2.2 Q Value Detection

Turn on the upper tube of the half-bridge driver to make the LC circuit store a certain amount of energy. Then, turn on the lower tube of the half-bridge driver to make the LC circuit self-oscillate and discharge to form a high-frequency exponentially attenuated oscillation.

The following figure shows the waveform.

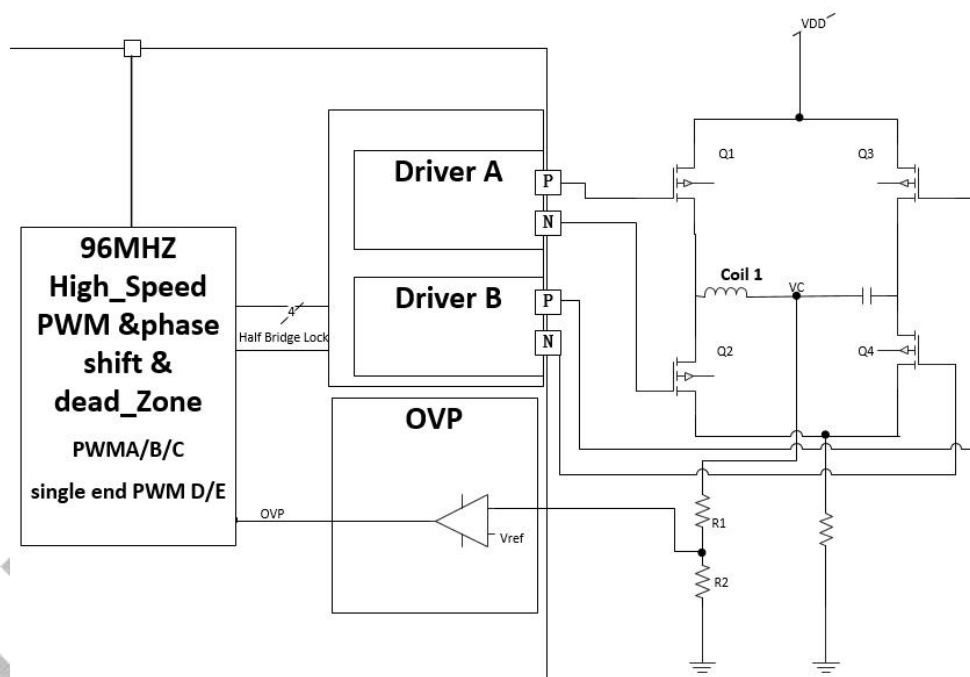


2.3 Ping Simulation

When the CV90367B sends a very short pulse to the LC, and the LC will oscillate. When there is an Rx device approaching, the oscillation amplitude of the LC will change, so that the Rx device is detected. Ping simulation can greatly decrease the average power consumption of Tx device in standby state.

2.4 Hardware Over-voltage Protection

The CV90367B has a built-in hardware over-voltage protection circuit. This circuit enables the chip to have a rapid protection trigger mechanism to avoid high voltage impact on the transmitter system components and receiver equipment due to anomalies (such as debris), which can cause the coil resonance voltage to be ultra high. The CV90367B has a triple over-voltage protection mechanism. The first stage is software protection. When the VC voltage reaches or approaches the protection voltage preset by the software, the software stops increasing the transmitting energy. When the VC voltage exceeds the R1/R2 divided voltage and is higher than the N-end voltage (3.3 V) of the comparator, the second-stage hardware protection mechanism is triggered, and the OVP will generate the Half-Bridge Lock signal, which locks the full-bridge driver working mode to half-bridge mode (Q3 is off and Q4 is normally on). At this time, the transmitting energy of the Tx device is halved, and the OVP interrupt is generated. If the Tx device normally receives the communication signal from the Rx device, the VC voltage does not continue to rise, and the software determines whether the system resumes normal charging. If the VC voltage continues to rise in the half-bridge working mode, the system will trigger the third-stage protection, turn off Q1 and Q3, and normally open Q2 and Q4. The MOSFET enters the discharge state.



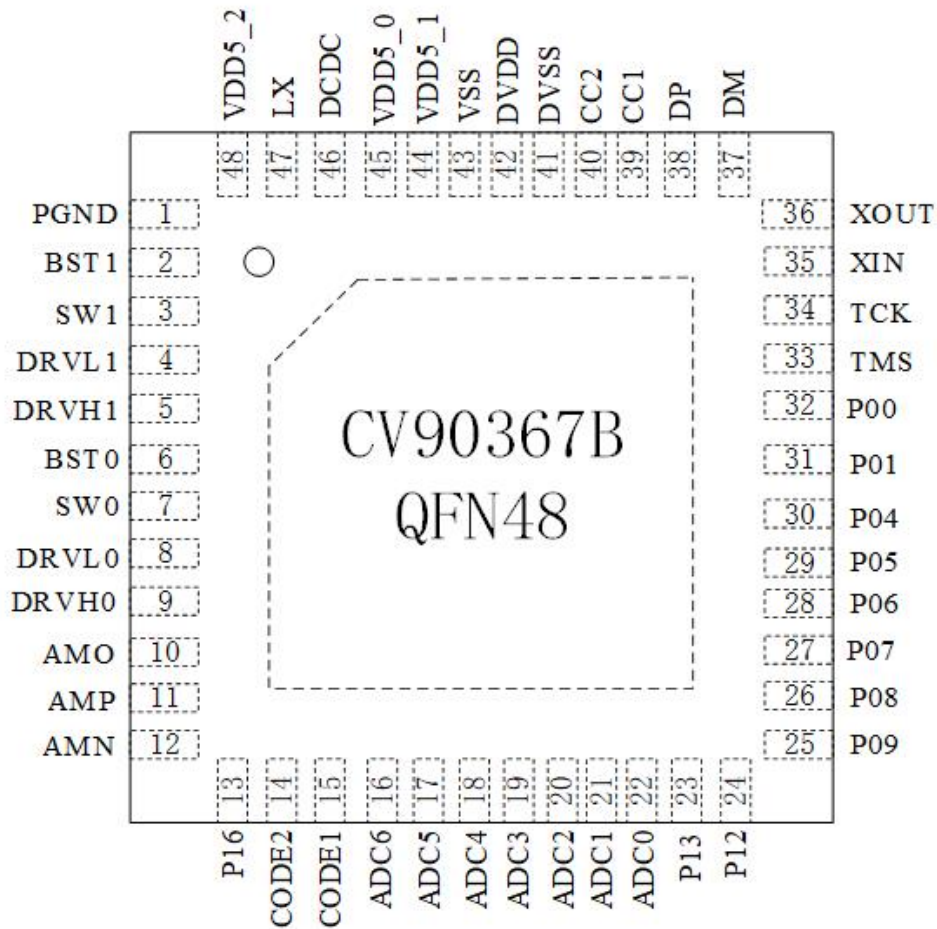
Block diagram of hardware protection circuit

2.5 Debris Detection

The CV90367B uses the Q value detection and power loss methods to detect debris, so as to make accurate and rapid judgment and protection:

- Q value detection: When the Q value detected by the Tx device is lower than the preset value, FOD alarm is generated quickly;

3 Pin Assignments



3.1 Pin Descriptions

Pin Number	Name	Description
1	PGND	Power Ground
2	BST1	MOSFET Half-Bridge Driver 1 High-side bootstrap supply
3	SW1	MOSFET Half-Bridge Driver 1 High-side source connection.
4	DRVL1	MOSFET Half-Bridge Driver 1 Low-Side output
5	DRVH1	MOSFET Half-Bridge Driver 1 High-Side output
6	BST0	MOSFET Half-Bridge Driver 0 High-side bootstrap supply
7	SW0	MOSFET Half-Bridge Driver 0 High-side source connection.
8	DRVL0	MOSFET Half-Bridge Driver 0 Low-Side output
9	DRVH0	MOSFET Half-Bridge Driver 0 High-Side output

Pin Number	Name	Description
10	AMO	Op-amp output terminal
11	AMP	Op-amp postive input terminal
12	AMN	Op-amp nagtive input terminal
13	P16	General-purpose digital I/O pin ADC
14	CODE2	Current sensing demodulation input
15	CODE1	Voltage sensing demodulation input
16	ADC6	ADC input channel 6
17	ADC5	ADC input channel 5
18	ADC4	ADC input channel 4
19	ADC3	ADC input channel 3
20	ADC2	ADC input channel 2
21	ADC1	ADC input channel 1
22	ADC0	ADC input channel 0
23	P13	General-purpose digital I/O pin
24	P12	General-purpose digital I/O pin
25	P09	General-purpose digital I/O pin
26	P08	General-purpose digital I/O pin
27	P07	General-purpose digital I/O pin
28	P06	General-purpose digital I/O pin
29	P05	General-purpose digital I/O pin
30	P04	General-purpose digital I/O pin
31	P01	General-purpose digital I/O pin
32	P00	General-purpose digital I/O pin
33	TMS	Emulation port data pin
34	TCK	Emulation port clock pin
35	XIN	External crystal input pin
36	XOUT	External crystal output pin

Pin Number	Name	Description
37	DM	USB D- interface
38	DP	USB D+ interface
39	CC1	Type-C CC1 detection pin
40	CC2	Type-C CC2 detection pin
41	DVSS	Ground
42	DVDD	VDD1.8V
43	VSS	Ground
44	VDD5_1	power supply
45	VDD5_0	power supply
46	DCDC	VIN power input
47	LX	DCDC output pin, connected to 6.8uH inductor
48	VDD5_2	power supply

4 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Voltage range	SW0, SW1	-0.3	30	V
	BST0, BST1	-0.3	36	V
	DRVL0, DRVL1	-0.3	6	V
	DRVH0, DRVH1	-0.3	36	V
	DVDD	-0.3	2	V
	PGND, DVSS, VSS	-0.3	0.3	V
	Other Pin	-0.3	6	V
Junction temperature	T_J		125	°C
Storage temperature	T_{stg}	-40	150	°C
Thermal resistance (junction temperature to environment)	θ_{JA}	47		°C/W
Human Body Model	ESD	-2000	2000	V

5 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply Voltage	V _{IN}	5.5		25	V
Input voltage	V _{DD}	0	5	5.5	V
	DV _{DD}	0	1.8	2	V
I/O voltage	CC1, CC2	0	5	5.5	V
	AMPIN, AMPIP, AMPOT, DP, DM	0	5	5.5	V
	P00—P06, P10—P17	0	5	5.5	V
	ADC0—ADC4, CODE1, CODE2	0	5	5.5	V
	AV _{DD} , nRST, XIN, XOUT, MDAT, MCLK	0	5	5.5	V
Standby power consumption	I _{standby}		10		mA
Operating temperature	T _A	-40		85	°C

6 Typical Applications Schematic

Please refer to page 11 of this article for a typical schematic.

7 Ordering Information

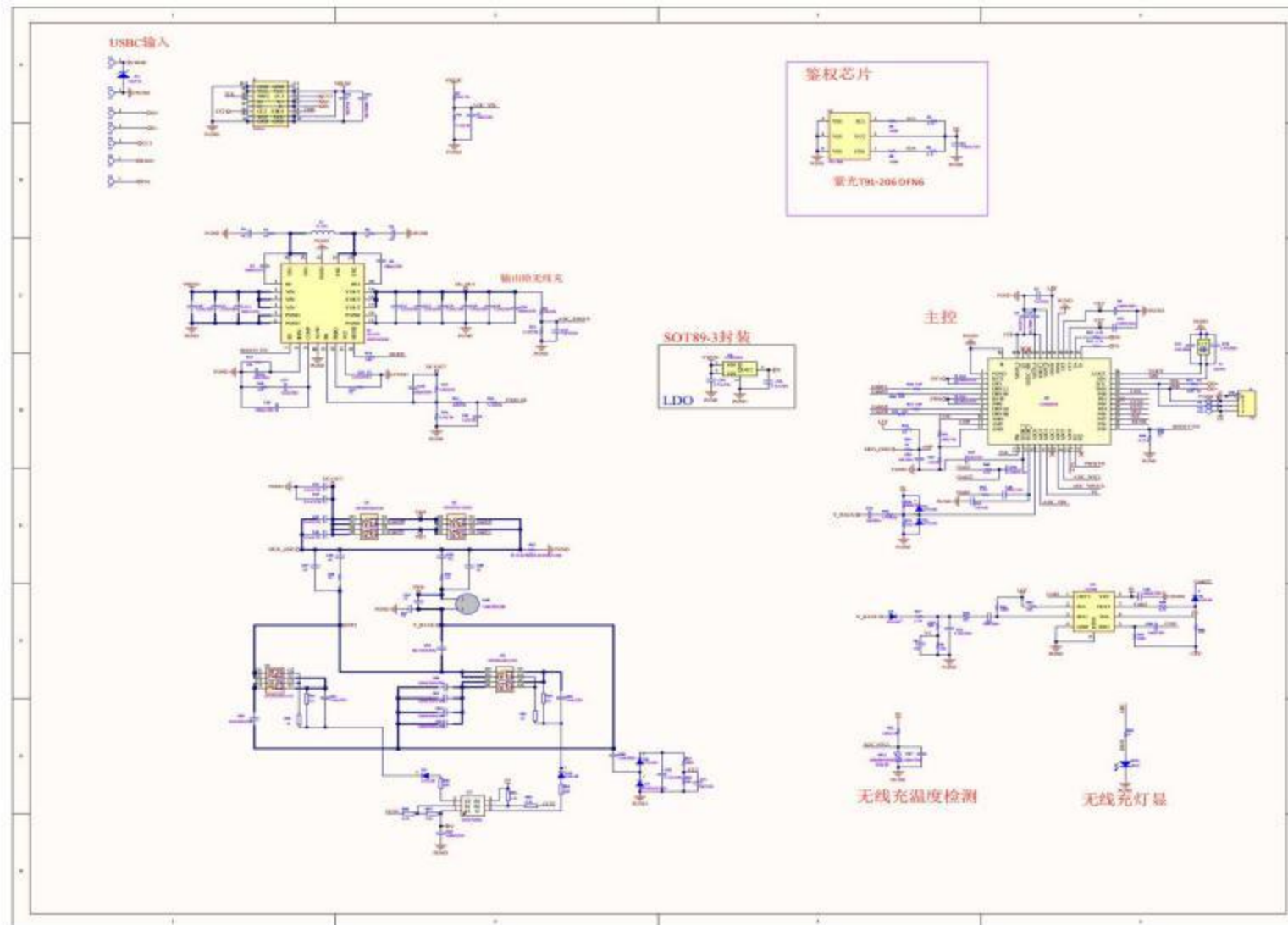
The package outline is shown on the page 12.

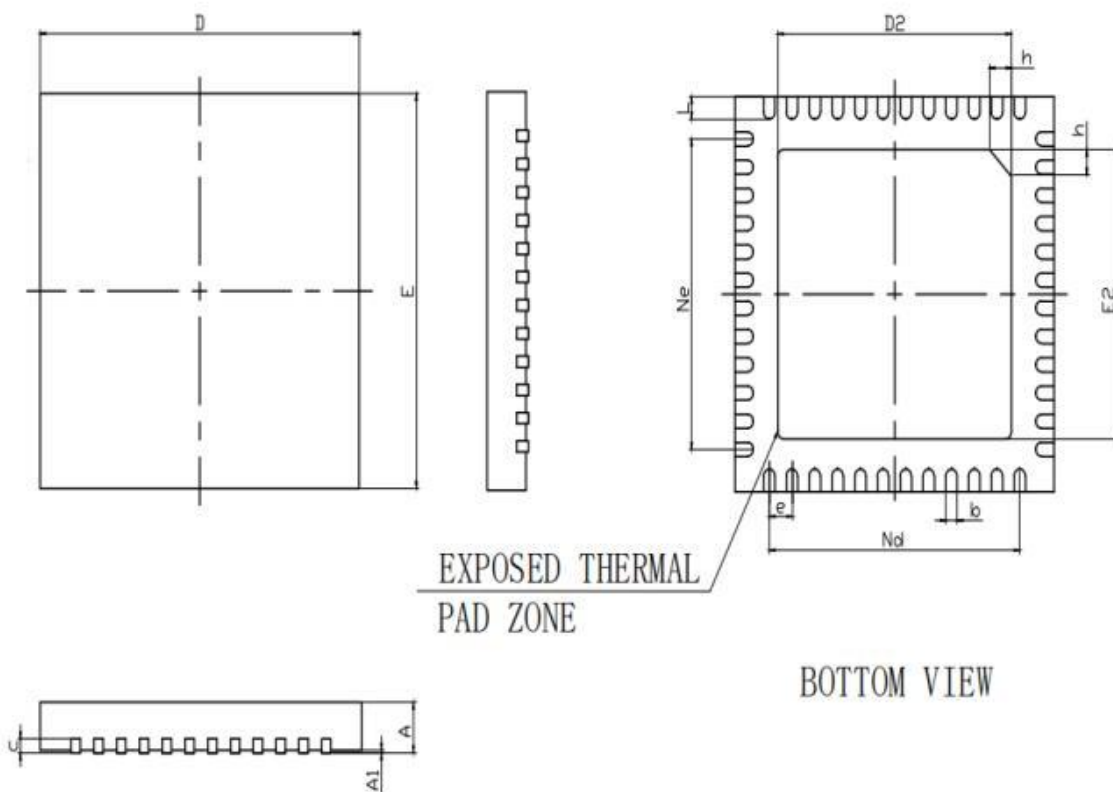
Part Number	Dimension	MSL Rating	Shipping Packaging	MPQ
CV90367B	QFN48 (6.00 * 6.00 * 0.75 mm)	MSL3	Reel	3000 PCS

8 Product Silkscreen Description



Position	Marking	Description
Line 1	CVSMicro	The Manufacturer
Line 2	CV90367B	The Part Number
Line 3	XXXXX	Lot Number





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.20	0.30
D	5.90	6.00	6.10
D2	4.3REF		
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.3REF		
L	0.35	0.40	0.45
h	0.35REF		

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