

Description

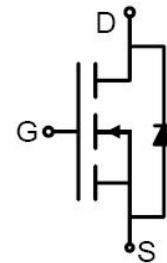
ELV686R6ND N-channel Enhancement Mode Power MOSFET

Features

68V, 80A
 $R_{DS(ON)} < 8.6\text{m}\Omega$ @ $V_{GS} = 10\text{V}$
 Advanced Trench Technology
 Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
 Lead free product is acquired

Application

Load Switch
 PWM Application
 Power management



TO-252-4R(DPAK) top view

Marking and pin Assignment

Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	TUBE (PCS)	Inner BOX (PCS)	Per Carton (PCS)
ELV686R6ND	ELV686R6ND	TAPING	TO-252-4R	13inch	2500	25000

Absolute Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		68	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_c = 25^\circ\text{C}$	80	A
		$T_c = 100^\circ\text{C}$	52	A
I_{DM}	Pulsed Drain Current ^{note1}		320	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		121	mJ
P_D	Power Dissipation	$T_c = 25^\circ\text{C}$	116	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.85	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	$^\circ\text{C}$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	68	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=68\text{V}$, $V_{GS}=0\text{V}$,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2	-	4	V
$R_{DS(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{GS}=10\text{V}$, $I_D=30\text{A}$	-	6.6	8.6	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	4062	-	pF
C_{oss}	Output Capacitance		-	261	-	pF
C_{rss}	Reverse Transfer Capacitance		-	231	-	pF
Q_g	Total Gate Charge	$V_{DS}=30\text{V}$, $I_D=20\text{A}$, $V_{GS}=10\text{V}$	-	35	-	nC
Q_{gs}	Gate-Source Charge		-	11	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	9	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=30\text{V}$, $I_D=20\text{A}$, $R_{\text{GEN}}=6\Omega$, $V_{GS}=10\text{V}$	-	15	-	ns
t_r	Turn-on Rise Time		-	94	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	46	-	ns
t_f	Turn-off Fall Time		-	32	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	80	-	A
I_{sM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	320	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_s=80\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$T_J=25^\circ\text{C}$ $I_F=20\text{A}, dI/dt=100\text{A}/\mu\text{s}$	-	78	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	51	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}$, $V_{DD}=35\text{V}$, $V_G=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=22\text{A}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

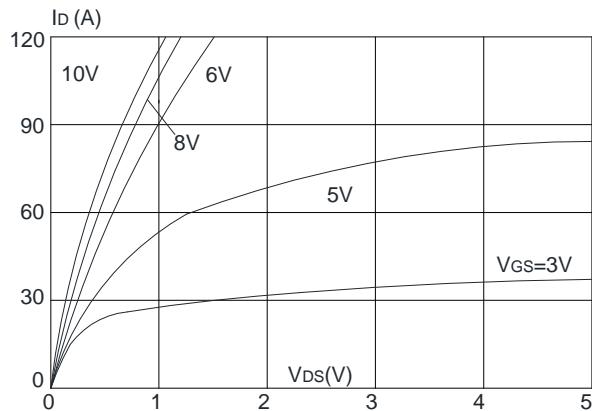


Figure 3: On-resistance vs. Drain Current

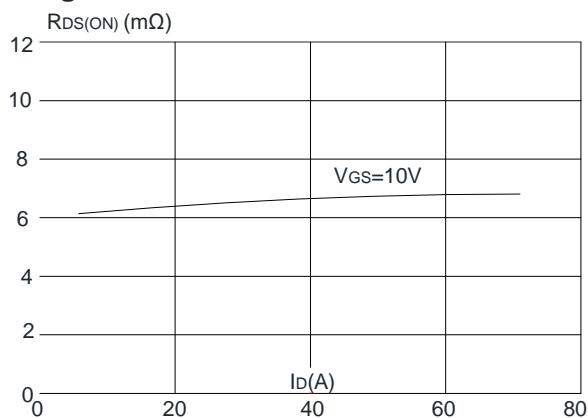


Figure 5: Gate Charge Characteristics

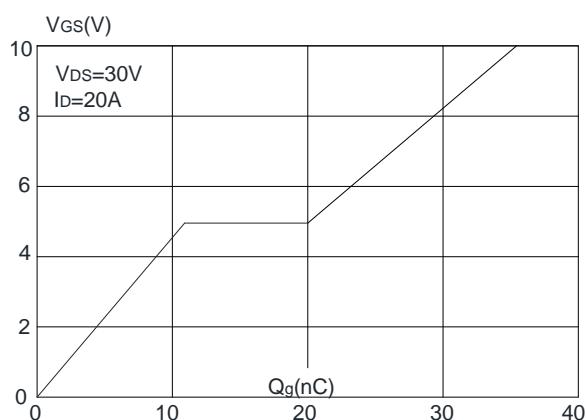


Figure 2: Typical Transfer Characteristics

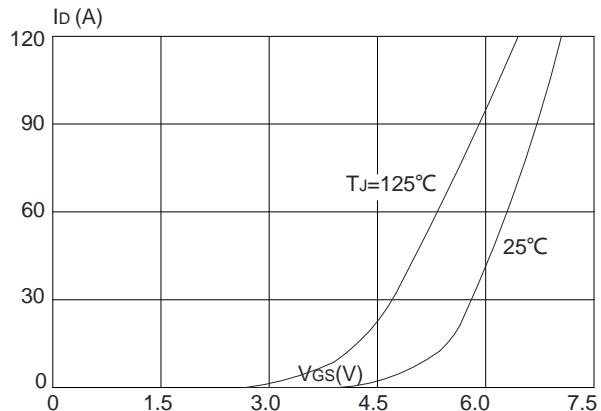


Figure 4: Body Diode Characteristics

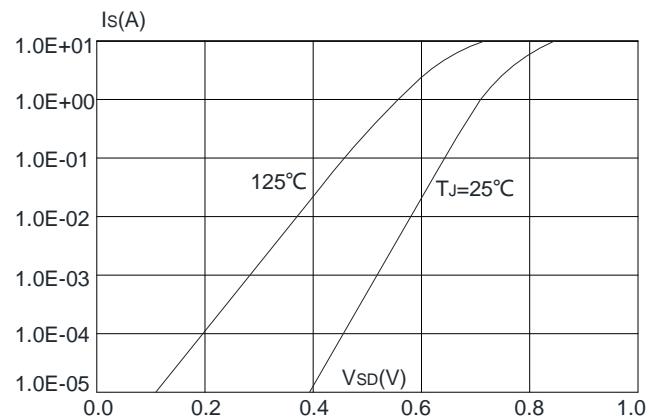


Figure 6: Capacitance Characteristics

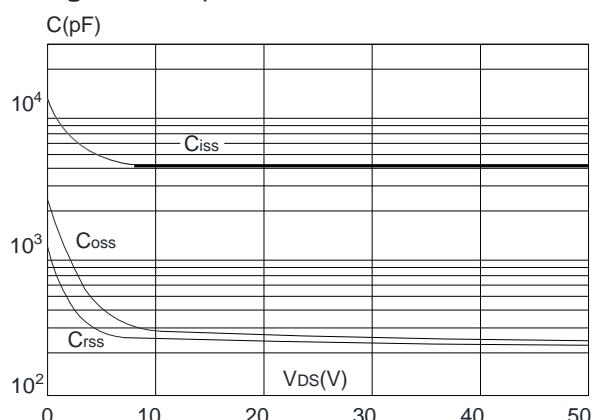


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

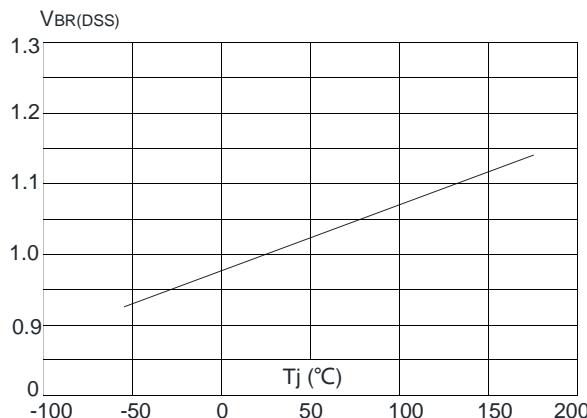


Figure 9: Maximum Safe Operating Area

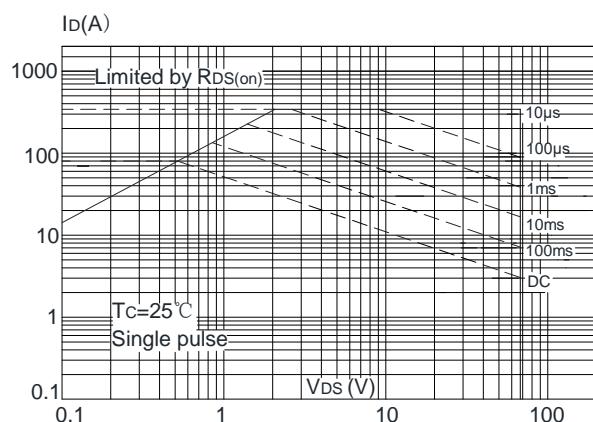


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

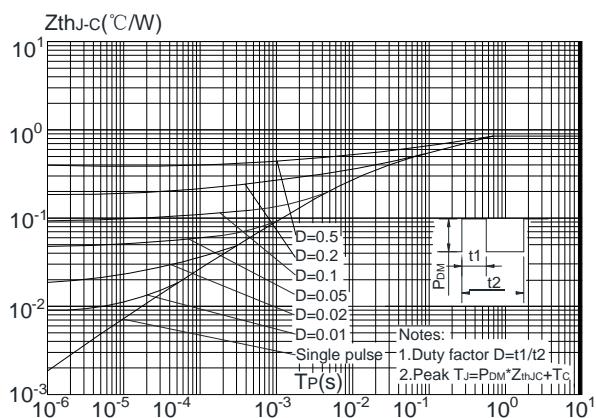


Figure 8: Normalized on Resistance vs. Junction Temperature

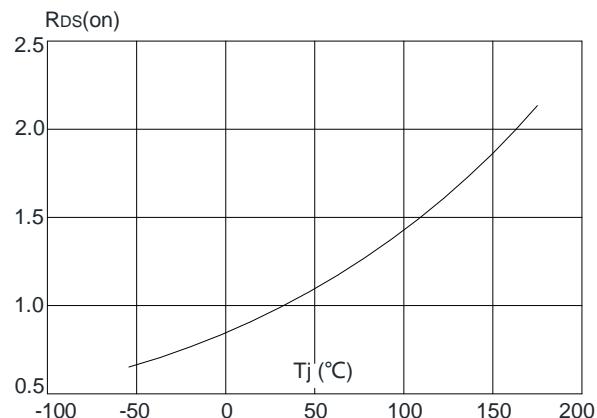
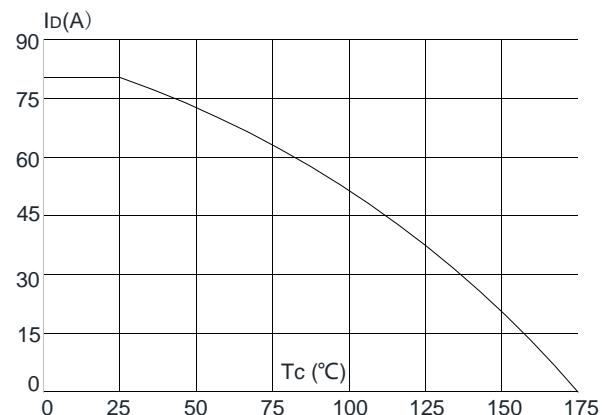


Figure 10: Maximum Continuous Drain Current vs. Case Temperature



Test Circuit

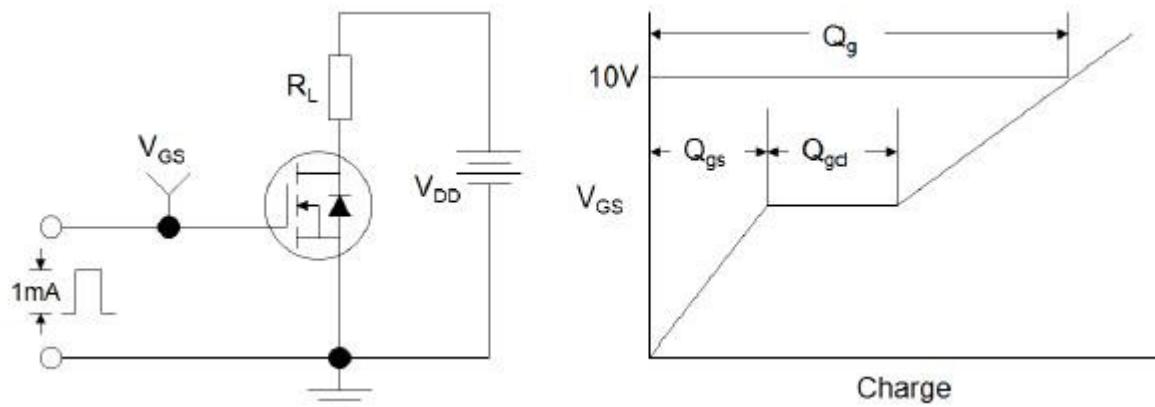


Figure 1:Gate Charge Test Circuit & Waveform

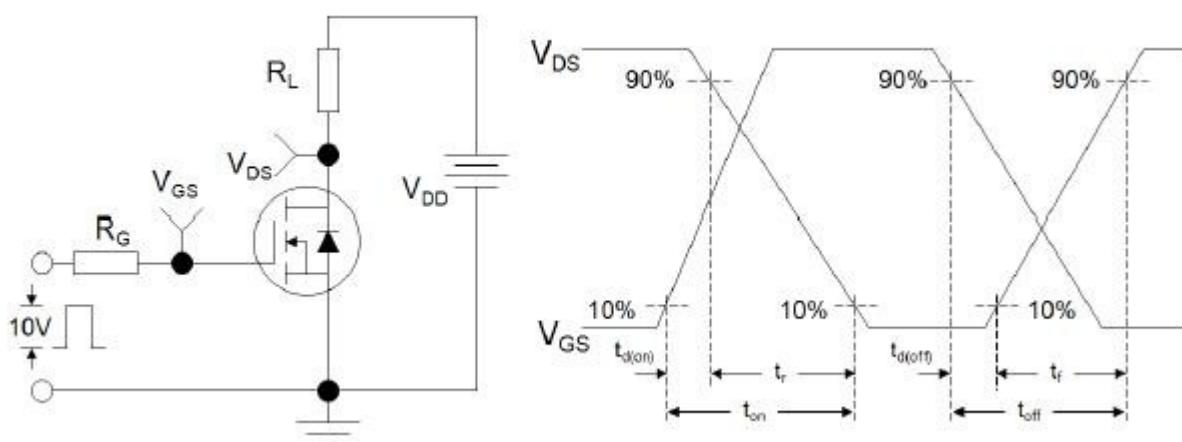


Figure 2: Resistive Switching Test Circuit & Waveforms

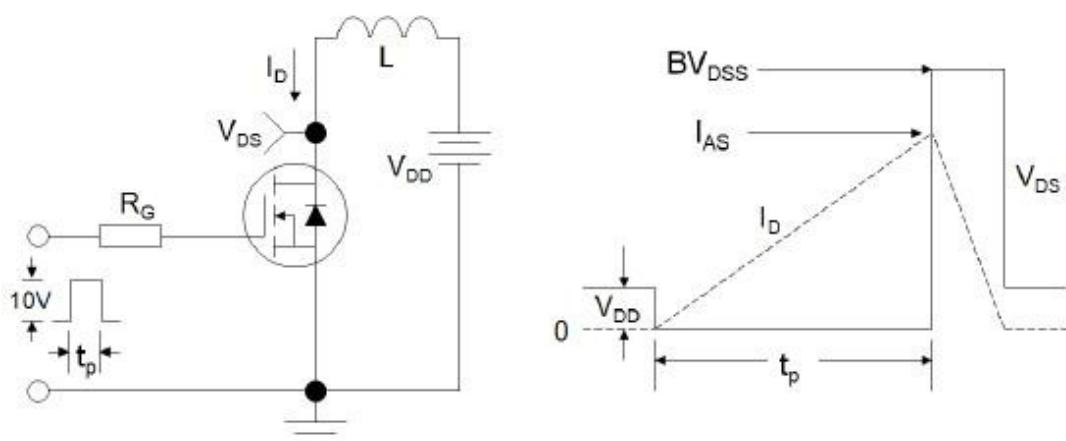
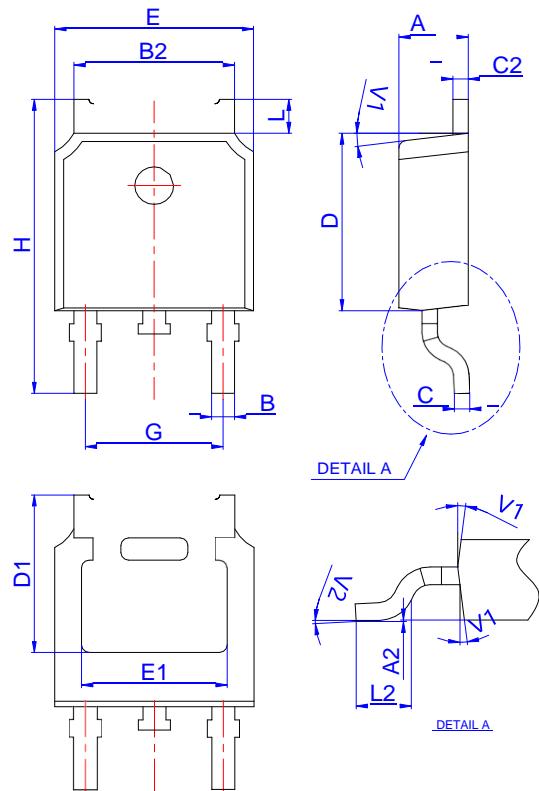


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

Package Mechanical Data-TO-252-4R



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Product Naming Rules

